DATA TRANSLATION

UM-16501-G

DT300 Series
User's Manual

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Radio and Television Interference

This equipment has been tested and found to comply with CISPR EN55022 Class A and EN50082-1 (CE) requirements and also with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Changes or modifications to this equipment not expressly approved by Data Translation could void your authority to operate the equipment under Part 15 of the FCC Rules.

Note: This product was verified to meet FCC requirements under test conditions that included use of shielded cables and connectors between system components. It is important that you use shielded cables and connectors to reduce the possibility of causing interference to radio, television, and other electronic devices.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Table of Contents

About this Manual

This manual describes the features of the DT300 Series boards, the capabilities of the DT300 Series Device Driver, and how to program the DT300 Series board using DT-Open Layers™ software. Troubleshooting and calibration information is also provided.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for using and/or programming the DT300 Series boards for data acquisition operations in Microsoft® Windows® 98, Windows Me (Millennium Edition), Windows NT® 4.0, Windows 2000, or Windows XP. It is assumed that you have some familiarity with data acquisition principles and that you understand your application.

What You Should Learn from this Manual

This manual provides detailed information about the features of the DT300 Series boards and the capabilities of the DT300 Series Device Driver. The manual is organized as follows:

- Chapter 1, "Overview," describes the major features of the board, as well as the supported software and accessories for the board.
- Chapter 2, "Principles of Operation," describes all of the board's features and how to use them in your application.
- Chapter 3, "Supported Device Driver Capabilities," lists the data acquisition subsystems and the associated features accessible using the DT300 Series Device Driver.
- Chapter 4, "Programming Flowcharts," describes the processes you must follow to program the subsystems on the DT300 Series board using DT-Open Layers-compliant software.

- Chapter 5, "Calibration," describes how to calibrate the analog I/O circuitry of the board.
- Chapter 6, "Troubleshooting," provides information that you can use to resolve problems with the board and the device driver, should they occur.
- Appendix A, "Specifications," lists the specifications of the board.
- Appendix B, "Connector Pin Assignments," shows the pin assignments for the connectors on the board and for the STP300 screw termination panel.
- An index completes this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information or information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.

Related Information

Refer to the following documents for more information on using the DT300 Series board:

- *DT300 Series Getting Started Manual* (UM-16503). This manual, provided on the Data Acquisition OMNI CD™, describes the how to install the DT300 Series board and related software.

- *DT Measure Foundry Getting Started Manual* (UM-19298) and online help. These documents describe how to use DT Measure Foundry to build drag-and-drop test and measurement applications for Data Translation® data acquisition boards without programming.
- *DataAcq SDK User's Manual* (UM-18326). For programmers who are developing their own application programs using the Microsoft C compiler, this manual describes how to use the DT-Open Layers™ Data Acq SDK to access the capabilities of Data Translation data acquisition boards. This manual is provided on the Data Acquisition OMNI CD.
- *DTx-EZ Getting Started Manual* (UM-15428). This manual describes how to use the ActiveX controls provided in DTx-EZ™ to access the capabilities of Data Translation's data acquisition boards in Microsoft® Visual Basic® or Visual C++®.
- *DT VPI User Manual* (UM-16150). This manual describes how to use DT VPI™ and the Agilent® VEE™ visual programming language to access the capabilities of Data Translation's data acquisition boards.
- *DT-LV Link Getting Started Manual* (UM-15790). This manual describes how to use DT-LV Link™ with the LabVIEW® graphical programming language to access the capabilities of Data Translation's data acquisition boards.
- *PCI Specification:* PCI Local Bus Specification, PCI Special Interest Group, Portland, OR. (Revision 2.1, June 1, 1995).
- Microsoft Windows 98, Windows Me, Windows NT 4.0, Windows 2000, or Windows XP documentation.

Where To Get Help

Should you run into problems installing or using a DT300 Series board, our Technical Support Department is available to provide technical assistance. Refer to Chapter 6 for more information. If you are outside the U.S. or Canada, call your local distributor, whose number is listed in your Data Translation product handbook.

1

Overview

Features

The DT300 Series is a family of low-cost, multifunction data acquisition boards for the PCI bus. The DT300 Series consists of the following boards: DT301, DT302, DT303, DT304, DT321, and DT322. These board types differ in analog I/O resolution, analog input sample frequency, analog input ranges, and the number of analog output channels, as shown in Table 1.

Table 1: Differences Among DT300 Series Boards

Board Type	Analog I/O Resolution	Analog Input Sample Frequency	Analog Input Ranges[a]	Analog Output Channels
DT301	12 bit	225 kHz	±10 V, 0 to 10 V	0
DT302	12 bit	225 kHz	±10 V, 0 to 10 V	2
DT303	12 bit	400 kHz	±10 V, 0 to 10 V	0
DT304	12 bit	400 kHz	±10 V, 0 to 10 V	2
DT321	16 bit	250 kHz	±10 V	0
DT322	16 bit	250 kHz	±10 V	2

a. Assumes a gain of 1. Using these ranges with gains of 2, 4, or 8 yields a number of effective input ranges; refer to page 12 for more information.

All DT300 Series board share the following major features:

- PCI bus mastering capability for analog inputs;
- 16 single-ended or pseudo-differential analog input channels, or 8 differential analog input channels;
- Signal conditioning through connections to 5B Series backplanes;
- Input gains of 1, 2, 4, and 8;
- Continuously-paced and triggered scan capability;

- A 1024-location channel-gain list that supports sampling analog input channels at the same or different gains in sequential or random order;
- Up to 256 scans per trigger for a total of 262,144 samples per trigger in triggered scan mode;
- Internal and external clock sources for the analog input subsystem;
- Digital TTL triggering for the analog input subsystem;
- Software calibration of the analog I/O circuitry;
- Two 8-bit digital ports programmable as inputs or outputs on a per-port basis; digital input lines from these lines can be included as part of the analog input channel-gain list to correlate the timing of analog and digital events; digital outputs can drive external solid-state relays;
- One 7-bit digital I/O port programmable as a general-purpose (non-clocked) input or output port;
- Four user counter/timers programmable for event counting, frequency measurement, rate generation (continuous pulse output), one-shot pulse output, and repetitive one-shot pulse output;
- Programmable gate types; and
- Programmable pulse output polarities (output types) and duty cycles.

For a discussion of these features in detail, refer to Chapter 2.

Supported Software

The following software is available for use with the DT300 Series board:

- **DT300 Series Device Driver** – This software is shipped on the Data Acquisition OMNI CD™. You *must* load the device driver to use the DT300 Series board with any of the supported software packages or utilities. Refer to the *DT300 Series Getting Started Manual* (UM-16504) for more information on loading the device driver.
- **The Quick Data Acq application** – This software is shipped on the Data Acquisition OMNI CD. The Quick Data Acq application provides a quick way to get a DT300 Series board up and running. Using the Quick Data Acq application, you can verify the features of the board, display data on the screen, and save data to disk. Refer to the *DT300 Series Getting Started Manual* (UM-16504) for information on using the Quick Data Acq application.
- **Scope application** – This software is shipped on the Data Acquisition OMNI CD. The Scope application emulates three basic instruments: a simple oscilloscope chart recorder, a data logger, and a multi-channel oscilloscope. Using the Scope application, you can monitor data online and capture it to disk. Refer to the online documentation provided on the CD-ROM for more information.
- **Calibration Utility** – This software is shipped on the Data Acquisition OMNI CD. This utility allows you to calibrate the analog I/O circuitry of the board. Refer to page 101 for more information on this utility.

- **DT Measure Foundry** – An evaluation version of this software is included on the Data Acquisition OMNI CD. DT Measure Foundry is drag-and-drop test and measurement application builder designed to give you top performance with ease-of-use development. Order the full development version of this software package to develop your own application using real hardware.
- **DataAcq SDK** – This software is shipped on the Data Acquisition OMNI CD. Use the Data Acq SDK if you want to use Windows 98, Windows Me, Windows NT 4.0, Windows 2000, or Windows XP to develop your own application software for the DT300 Series boards using the Microsoft C compiler; the DataAcq SDK complies with the DT-Open Layers standard.
- **DTx-EZ** – Order this optional software package if you want to use ActiveX controls to access the capabilities of the DT300 Series boards using Microsoft Visual Basic or Visual C++; DTx-EZ complies with the DT-Open Layers standard.
- **DT VPI** – Order this optional software package if you want to use the Aglient VEE visual programming language to access the capabilities of the DT300 Series boards.
- **DT-LV Link** – Order this optional software package if you want to use the LabVIEW graphical programming language to access the capabilities of the DT300 Series boards.
- **Testpoint** – Order this optional software package if you want use a drag-and-drop software environment for designing test, measurement, and data acquisition applications.

Refer to Data Translation's data acquisition catalog for information about selecting the right software package for your needs.

Accessories

The following optional accessories are available for the DT300 Series board:

- **STP300 screw terminal panel** – Screw terminal panel with two connectors. Connector J1 accommodates the analog and digital I/O signals from the DT300 Series board, and connector J2 allows you to connect 5B signal conditioning backplanes.
- **STP68 screw terminal panel** – A generic, 68-pin screw terminal panel that has one connector to accommodate the signals provided on connector J1 of the DT300 Series boards.
- **STP68-DIN screw terminal panel** – A generic, 68-pin screw terminal panel that is DIN-rail mountable. This screw terminal panel has one connector to accommodate the signals provided on connector J1 of the DT300 Series boards.
- **EP305 cable** – A 2-meter, twisted-pair, shielded cable that connects the 68-pin connector (J1) on the DT300 Series board to the J1 connector on the STP300 screw terminal panel.
- **5B01 or 5B08 backplane and 5B modules** – The 5B01 is a 16-channel backplane; the 5B08 is an 8-channel backplane. Both backplanes accept 5B modules for signal conditioning applications, including measuring thermocouples, RTDs, voltage input, current input, strain gage input, and frequency input. The 5B01, when used with the STP300, also provides two analog output channels for isolated 4 to 20 mA analog output modules.
- **AC1315 cable** – A 2-foot cable with a 26-pin connector on each end that connects a 5B signal conditioning backplane to connector J2 on the STP300 screw terminal panel.
- **DC300 backshell connector kit** – This kit includes a 68-pin mating connector and backshell if you want to build your own cable.

2

Principles of Operation

This chapter describes the analog input, analog output, digital I/O, and counter/timer features of the DT300 Series board. To frame the discussions, refer to the block diagram shown in Figure 1. Note that bold entries indicate signals you can access.

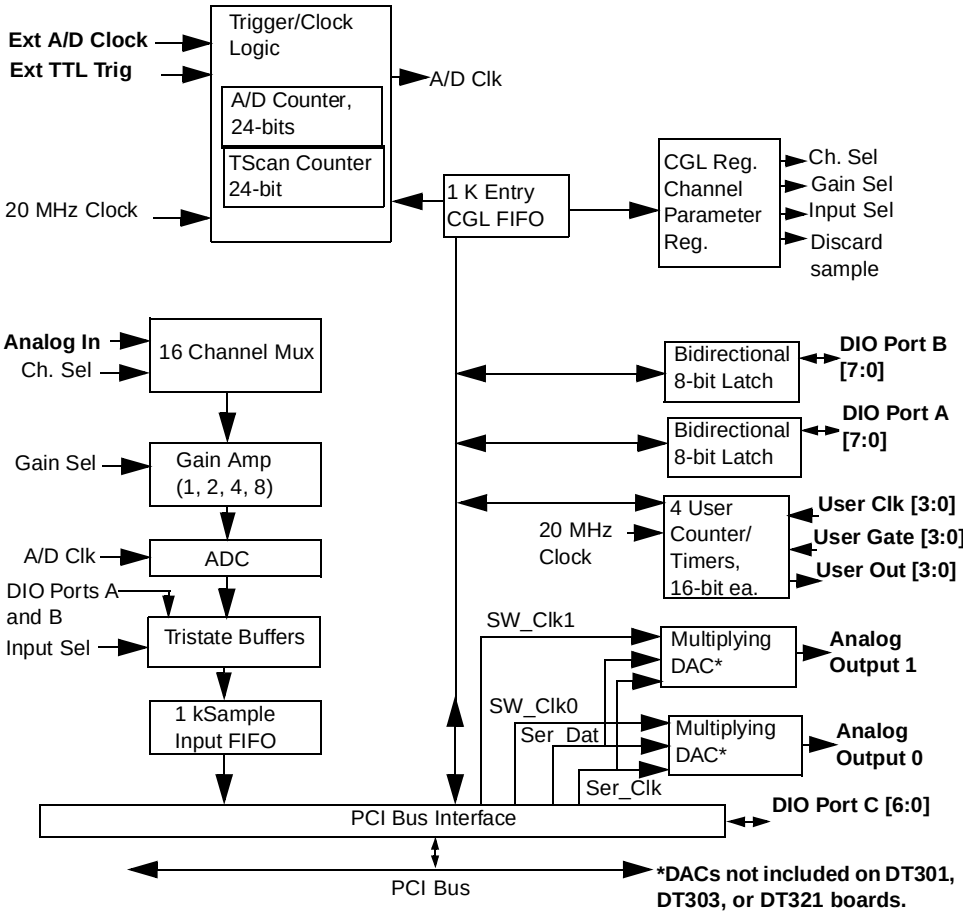


Figure 1: Block Diagram of the DT300 Series Boards

Analog Input Features

This section describes the features of the analog input (A / D) subsystem, including the following:

- Input resolution,
- Analog input channels,
- Input ranges and gains,
- A / D sample clock sources,
- Analog input conversion modes,
- Trigger sources and trigger acquisition modes,
- Data formats and transfer, and
- Error conditions.

Input Resolution

Table 2 lists the input resolutions supported by the DT300 Series boards. The resolution is fixed for each board type; therefore, it cannot be programmed in software.

Table 2: Supported Analog Input Resolutions

Board Type	Supported Resolution
DT301	12 bits
DT302	12 bits
DT303	12 bits
DT304	12 bits
DT321	16 bits
DT322	16 bits

Analog Input Channels

The DT300 Series board supports 16 single-ended or pseudo-differential analog input channels, or 8 differential analog input channels on board. Refer to the *DT300 Series Getting Started Manual* for a description of how to wire these signals. You configure the channel type through software.

Note: For pseudo-differential inputs, specify single-ended in software; in this case, how you wire these signals determines the configuration.

The DT300 Series board can acquire data from a single analog input channel or from a group of analog input channels. Onboard channels are numbered 0 to 15 for single-ended and pseudo-differential inputs or 0 to 7 for differential inputs. The following subsections describe how to specify the channels.

Specifying a Single Channel

The simplest way to acquire data from a single channel is to specify the channel for a single-value analog input operation using software; refer to page 16 for more information on single-value operations.

You can also specify a single channel using the analog input channel list, described in the next section.

Specifying One or More Channels

On the DT300 Series board, you can read data from one or more analog input channels using an analog input channel list. You can group the channels in the list sequentially (either starting with 0 or with any other analog input channel) or randomly. You can also specify a single channel or the same channel more than once in the list.

Using software, specify the channels in the order you want to sample them. The analog input channel list corresponds to the Channel-Gain List FIFO (first-in, first-out buffer) on the board. You can enter up to 1,024 entries in the channel list. The channels are read in order (using continuous paced mode or triggered scan mode) from the first entry to the last entry in the channel list. You can read the channels in the channel list up to 256 times per trigger (for a total of 262,144 samples per trigger) using triggered scan mode. Refer to page 16 for more information on the supported conversion modes.

If you wish, you can also use software to set up a channel inhibit list. This feature is useful if you want to discard acquired values from specific entries in the channel list. Using the channel inhibit list, you can enable or disable inhibition for each entry in the analog input channel list. If enabled, the value is discarded after the channel is read; if disabled, the value is not discarded after the channel is read.

Specifying Digital Input Lines in the Analog Input Channel List

In addition to the analog input channels, the DT300 Series board allows you to read 16 digital I/O lines (Port A, lines 0 to 7 and Port B, lines 0 to 7) using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog and digital events.

To read these 16 digital I/O lines, specify channel 16 in the analog input channel list. You can enter channel 16 anywhere in the list and can enter it more than once, if desired.

Note: If channel 16 is the only channel in the channel-gain list, the board can read this channel at a rate of 3 MSamples/s.

The digital channel is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for these digital I/O lines, if you specify them in this manner.

Input Ranges and Gains

Each channel on the DT301, DT302, DT303, and DT304 board can measure unipolar and bipolar analog input signals, while each channel on the DT321 and DT322 board can measure bipolar analog input signals only. A unipolar signal is always positive (0 to 10 V on a DT300 Series board), while a bipolar signal extends between the negative and positive peak values (±10 V on a DT300 Series board).

Through software, specify the range as 0 to 10 V for unipolar signals or –10 V to +10 V for bipolar signals. Note that you specify the range for the entire analog input subsystem, not the range per channel.

DT300 Series boards provide gains of 1, 2, 4, and 8, which are programmable per channel. Table 3 lists the effective ranges supported by the DT300 Series board using these gains.

Table 3: Gains and Effective Ranges

Gain	Unipolar Analog Input Range	Bipolar Analog Input Range[a]
1	0 to 10 V	±10 V
2	0 to 5 V	±5 V
4	0 to 2.5 V	±2.5 V
8	0 to 1.25 V	±1.25 V

a. DT321 and DT322 boards support bipolar analog input ranges only.

For each channel, choose the gain that has the smallest effective range that includes the signal you want to measure. For example, if the range of your analog input signal is ±1.5V, specify a range of –10 V to +10 V for the board and use a gain of 4 for the channel; the effective input range for this channel is then ±2.5V, which provides the best sampling accuracy for that channel.

The way you specify gain depends on how you specified the channels, as described in the following subsections.

Specifying the Gain for a Single Channel

The simplest way to specify the gain for a single channel is to specify the gain for a single-value analog input operation using software; refer to page 16 for more information on single-value operations.

You can also specify the gain for a single channel using an analog input gain list, described in the next section.

Specifying the Gain for One or More Channels

For DT300 Series boards, you can specify the gain for one or more analog input channels using an analog input gain list. Using software, set up the gain list by specifying the gain for each entry in the channel list. The gain list parallels the channel list. (The two lists together are often referred to as the channel-gain list.)

For example, assume the analog input channel list contains three entries: channels 5, 6, and 7; the gain list might look like this: 2, 4, 1, where a gain of 2 corresponds to channel 5, a gain of 4 corresponds to channel 6, and a gain of 1 corresponds to channel 7.

Note: For analog input channel 16 (the 16 digital I/O lines) in the channel list, specify a gain of 1 in the gain list.

A/D Sample Clock Sources

The DT300 Series board provides two clock sources for pacing analog input operations in continuous mode:

- An internal A/D sample clock that uses the 24-bit A/D Counter on the board; and
- An external A/D sample clock that you can connect to the screw terminal panel.

You use an A/D sample clock to pace the acquisition of each channel in the channel-gain list; this clock is also called the A/D pacer clock.

Note: If you enter digital I/O channel 16 in the channel-gain list, the A/D sample clock (internal or external) also paces the acquisition of the 16 digital input lines.

The following subsections describe the internal and external A / D sample clocks in more detail.

Internal A/D Sample Clock

The internal A / D sample clock uses a 20 MHz time base. Conversions start on the falling edge of the counter output; the output pulse is active low.

Using software, specify the clock source as internal and the clock frequency at which to pace the operation. The minimum frequency supported is 1.2 Hz (1.2 Samples / s); the maximum frequency supported differs depending on the board type, as shown in Table 4.

Table 4: Maximum Frequency Supported

Board Type	Maximum Frequency
DT301	225 kHz
DT302	225 kHz
DT303	400 kHz
DT304	400 kHz
DT321	250 kHz
DT322	250 kHz

According to sampling theory (Nyquist Theorem), specify a frequency that is at least twice as fast as the input's highest frequency component. For example, to accurately sample a 20 kHz signal, specify a sampling frequency of at least 40 kHz. Doing so avoids an error condition called *aliasing*, in which high frequency input components erroneously appear as lower frequencies after sampling.

Note: If your channel-gain list contains only digital input channel 16, the maximum frequency is 3 MHz (3 MSamples/s).

External A/D Sample Clock

The external A/D sample clock is useful when you want to pace acquisitions at rates not available with the internal A/D sample clock or when you want to pace at uneven intervals.

Connect an external A/D sample clock to screw terminal TB48 on the STP300 screw terminal panel (pin 22 on connector J1). Conversions start on the falling edge of the external A/D sample clock input signal.

Using software, specify the clock source as external. For the DT300 Series board, the clock frequency is always equal to the frequency of the external A/D sample clock input signal that you connect to the board through the screw terminal panel.

Analog Input Conversion Modes

DT300 Series boards support the following conversion modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. Using software, you can specify the range, gain, and analog input channel (among other parameters); acquire the data from that channel; and convert the result. The data is returned immediately. For a single-value operation, you cannot specify a clock source, trigger source, trigger acquisition mode, scan mode, or buffer.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Scan mode** takes full advantage of the capabilities of the DT300 Series boards. In a scan, you can specify a channel-gain list, clock source, trigger source, trigger acquisition mode, scan mode, buffer, and buffer wrap mode using software. Two scan modes are supported: continuously-paced scan mode and triggered scan mode (often called burst mode). These modes are described in the following subsections.

  Using software, you can stop a scan by performing either an orderly stop or an abrupt stop. In an orderly stop, the board finishes acquiring the specified number of samples, stops all subsequent acquisition, and transfers the acquired data to host memory; all subsequent triggers or retriggers are ignored. In an abrupt stop, the board stops acquiring samples immediately; the acquired data is not transferred to host memory, but all subsequent triggers or retriggers are ignored.

Continuously-Paced Scan Mode

Use continuously-paced scan mode if you want to accurately control the period between conversions of individual channels in a scan.

When it detects an initial trigger, the board cycles through the channel-gain list, acquiring and converting the value for each entry in the channel list (this process is defined as the scan). The board then wraps to the start of the channel-gain list and repeats the process continuously until either the allocated buffers are filled or until you stop the operation. Refer to page 30 for more information on buffers.

The conversion rate is determined by the frequency of the A/D sample clock; refer to page 14 for more information on the A/D sample clock. The sample rate, which is the rate at which a single entry in the channel-gain list is sampled, is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list.

To select continuously-paced scan mode, use software to specify the dataflow as continuous, continuous pre-trigger, or continuous about-trigger. The initial trigger source depends on the trigger acquisition mode you use. Refer to page 22 for more information on the supported trigger sources and trigger acquisition modes.

Triggered Scan Mode

DT300 Series boards support two triggered scan modes: internally-retriggered and externally-retriggered. These modes are described in the following subsections.

Internally-Retriggered Scan Mode

Use internally-retriggered scan mode if you want to accurately control both the period between conversions of individual channels in a scan and the period between each scan. This mode is useful when synchronizing or controlling external equipment, or when acquiring a buffer of data on each trigger or retrigger. Using this mode, you can acquire up to 262,144 samples per trigger (256 times per trigger x 1024-location channel-gain list).

When it detects an initial trigger, the DT300 Series board scans the channel-gain list a specified number of times (up to 256), then waits for an internal retrigger to occur. When it detects an internal retrigger, the board scans the channel-gain list the specified number of times, then waits for another internal retrigger to occur. The process repeats continuously until either the allocated buffers are filled or until you stop the operation; refer to page 30 for more information on buffers.

The sample rate is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list; refer to page 14 for more information on the A/D sample clock. The conversion rate of each scan is determined by the frequency of the internal retrigger clock. The internal retrigger clock is the Triggered Scan Counter on the board; the Triggered Scan Counter is a 24-bit counter with a 20MHz clock.

Using software, specify the frequency of the internal retrigger clock. The minimum retrigger frequency is 1.2 Hz (1.2 Samples/s). Table 5 lists the maximum retrigger frequency supported by the DT300 Series boards.

Table 5: Maximum Retrigger Frequency

Board	Maximum Retrigger Frequency
DT301/302	155 kHz
DT303/304	219 kHz
DT321/322	165 kHz

The appropriate *retrigger frequency* depends on a number of factors, determined by the following equations:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries} \times \text{\# of CGLs per trigger}}{\text{A/D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

For example, if you are using 16 channels in the channel-gain list (CGL), scanning the channel-gain list 256 times every trigger or retrigger, and using an A/D sample clock with a frequency of 100 kHz, set the maximum retrigger frequency to 24.41 Hz, since

$$24.41\ \text{Hz} = \frac{1}{\frac{(16 * 256)}{100\ \text{kHz}} + 2\ \mu s}$$

To select internally-retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous, continuous pre-trigger, or continuous about-trigger;
- Triggered scan mode usage as enabled;
- The retrigger mode as internal;
- The number of times to scan per trigger or retrigger (also called the multiscan count); and
- The frequency of the retrigger clock.

The initial trigger source depends on the trigger acquisition mode you use; refer to page 22 for more information on the supported and trigger sources and trigger acquisition modes.

Externally-Retriggered Scan Mode

Use externally-retriggered scan mode if you want to accurately control the period between conversions of individual channels and retrigger the scan based on an external event. Like internal retrigger scan mode, this mode allows you to acquire 262,144 samples per trigger (256 times per trigger x 1024-location channel-gain list).

Note: Use externally-retriggered scan mode with continuous post-trigger acquisitions only; refer to page 22 for more information on post-trigger acquisitions.

When a DT300 Series board detects an initial trigger (post-trigger source only), the board scans the channel-gain list up to 256 times, then waits for an external retrigger to occur. You can specify any supported post-trigger source as the initial trigger. Specify the external digital (TTL) trigger for the retrigger.

When the retrigger occurs, the board scans the channel-gain list the specified number of times, then waits for another external retrigger to occur. The process repeats continuously until either the allocated buffers are filled (if buffer wrap mode is none) or until you stop the operation (if buffer wrap mode is single or multiple); refer to page 30 for more information on buffers.

The conversion rate of each channel is determined by the frequency of the A / D sample clock; refer to page 14 for more information on the A / D sample clock. The conversion rate of each scan is determined by the period between external retriggers; therefore, it cannot be accurately controlled. The board ignores external triggers that occur while it is acquiring data. Only external retrigger events that occur when the board is waiting for a retrigger are detected and acted on.

To select externally-retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous (post-trigger);
- The triggered scan mode usage as enabled;
- The retrigger mode as an external retrigger (retrigger extra for DataAcq SDK users);
- The number of times to scan per trigger or retrigger (also called the multiscan count); and
- The retrigger source as the external digital (TTL) trigger.

Note: For DataAcq SDK users, if you want to use the same trigger source as both the initial trigger and the retrigger source, specify the external digital trigger as the initial trigger source and specify the retrigger mode as scan-per-trigger. In this case, you need not specify the retrigger source; the board uses the initial trigger source as the retrigger source.

Triggers

A trigger is an event that occurs based on a specified set of conditions. The DT300 Series boards support a number of trigger sources and trigger acquisition modes, described in the following subsections.

Trigger Sources

The DT300 Series board supports a software trigger and an external digital (TTL) trigger.

A software trigger event occurs when you start the analog input operation (the computer issues a write to the board to begin conversions). Specify the software trigger source in software.

An external digital trigger event occurs when the DT300 Series board detects either a rising or falling edge on the External TTL Trigger input signal connected to screw terminal TB46 on the STP300 screw terminal panel (pin 56 of connector J1). The trigger signal is TTL-compatible. Using software, specify the trigger source as a rising-edge external digital trigger (external for DataAcq SDK users) or falling-edge external digital trigger (extra for DataAcq SDK users).

Trigger Acquisition Modes

DT300 Series boards can acquire data in post-trigger mode, pre-trigger mode, or about-trigger mode. These trigger acquisition modes are described in more detail in the following subsections.

Post-Trigger Acquisition

Use post-trigger acquisition mode (continuous mode) when you want to acquire data when a post-trigger or retrigger, if using triggered scan mode, occurs.

Using software, specify

- The dataflow as continuous, and
- The trigger source to start the post-trigger acquisition (the post-trigger source) as any of the supported trigger sources.

Refer to page 16 for more information on the supported conversion modes; refer to page 22 for information on the supported trigger sources.

Post-trigger acquisition starts when the board detects the post-trigger event and stops when the specified number of post-trigger samples has been acquired or when you stop the operation.

If you are using triggered scan mode, the board continues to acquire post-trigger data using the specified retrigger source to clock the operation. Refer to page 18 for more information on triggered scan mode.

Figure 2 illustrates continuous post-trigger mode using a channel-gain list with three entries: channel 0, channel 1, and channel 2. Triggered scan mode is disabled. In this example, post-trigger analog input data is acquired on each clock pulse of the A/D sample clock. When it reaches the end of the channel-gain list, the board wraps to the beginning of the channel-gain list and repeats this process. Data is acquired continuously (continuously-paced scan mode).

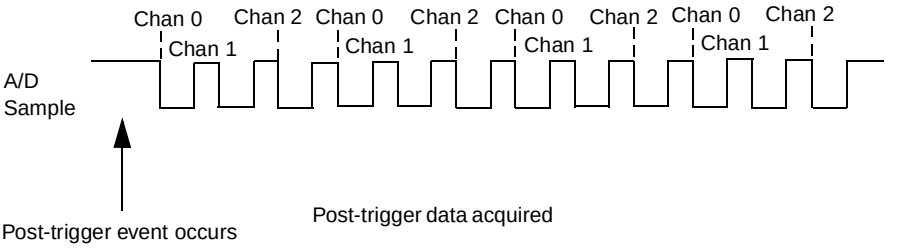


Figure 2: Continuous Post-Trigger Mode without Triggered Scan

Figure 3 illustrates the same example using triggered scan mode (either internally or externally retriggered). The multiscan count is 2, indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, post-trigger analog input data is acquired on each clock pulse of the A/D sample clock until the channel-gain list has been scanned twice; then, the board waits for the retrigger event. When the retrigger event occurs, the board scans the channel-gain list twice more, acquiring data on each pulse of the A/D sample clock. The process repeats continuously with every specified retrigger event.

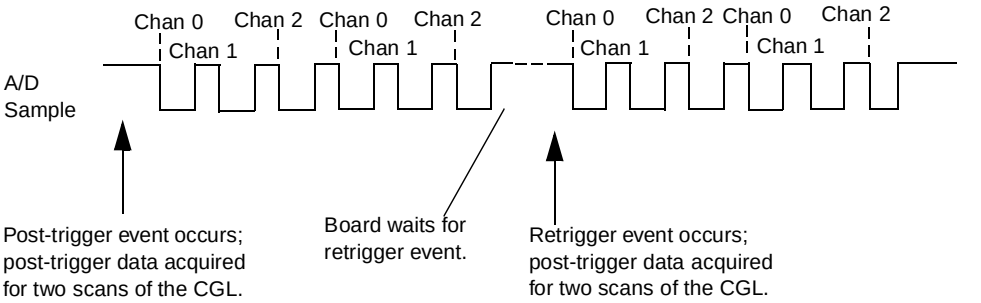


Figure 3: Continuous Post-Trigger Mode with Triggered Scan

Pre-Trigger Acquisition

Use pre-trigger acquisition mode (continuous pre-trigger mode) when you want to acquire data before a specific external event occurs.

Using software, specify

- The dataflow as continuous pre-trigger,
- The pre-trigger source as the software trigger,
- The post-trigger source as the external digital (TTL) trigger, and
- If you are using triggered scan mode, the retrigger mode as the internal retrigger.

Refer to page 16 for more information on the supported conversion modes; refer to page 22 for information on the supported trigger sources.

Note: When using pre-trigger acquisition, you cannot use externally-retriggered scan mode; refer to page 18 for more information on triggered scan mode.

Pre-trigger acquisition starts when you start the operation and stops when the board detects the selected post-trigger source, indicating that the first post-trigger sample was acquired (this sample is ignored).

If you are using internally-retriggered scan mode and the post-trigger event has not occurred, the board continues to acquire pre-trigger data using the internal retrigger clock to clock the operation. When the post-trigger event occurs, acquisition stops. Refer to page 18 for more information on internally-retriggered scan mode.

Figure 4 illustrates continuous pre-trigger mode using a channel-gain list of three entries: channel 0, channel 1, and channel 2. In this example, pre-trigger analog input data is acquired on each clock pulse of the A/D sample clock. When it reaches the end of the channel-gain list, the board wraps to the beginning of the channel-gain list and repeats this process. Data is acquired continuously until the post-trigger event occurs. When the post-trigger event occurs, acquisition stops.

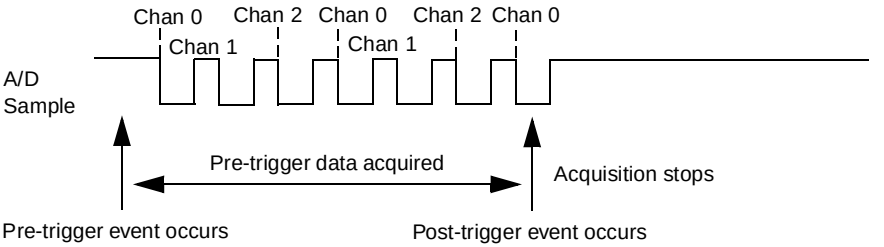


Figure 4: Continuous Pre-Trigger Mode

Figure 5 illustrates the same example using internally-retriggered scan mode. The multiscan count is 2, indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, pre-trigger analog input data is acquired on each clock pulse of the A/D sample clock until the channel-gain list has been scanned twice; then, the board waits for the internal retrigger event. When the internal retrigger occurs, the process repeats. Acquisition stops when the post-trigger event occurs.

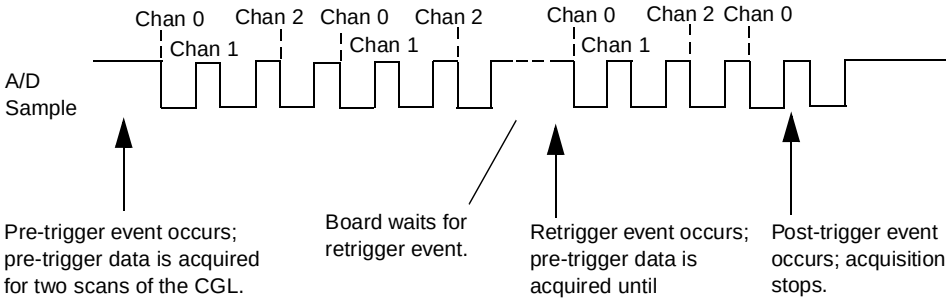


Figure 5: Continuous Pre-Trigger Mode with Triggered Scan

About-Trigger Acquisition

Use about-trigger acquisition mode (continuous about-trigger mode) when you want to acquire data both before and after a specific external event occurs. This operation is equivalent to doing both a pre-trigger and a post-trigger acquisition.

Using software, specify

- The dataflow as continuous about-trigger,
- The pre-trigger source as the software trigger,
- The post-trigger source as the external digital (TTL) trigger, and
- If you are using triggered scan mode, the retrigger mode as the internal retrigger.

Refer to page 16 for more information on the supported conversion modes; refer to page 22 for information on the supported trigger sources.

Note: When using about-trigger acquisition, you cannot use externally-retriggered scan mode; refer to page 18 for more information on triggered scan mode.

The about-trigger acquisition starts when you start the operation. When it detects the selected post-trigger event, the board stops acquiring pre-trigger data and starts acquiring post-trigger data.

If you are using internally-retriggered scan mode and the post-trigger event has not occurred, the board continues to acquire pre-trigger data using the internal retrigger clock to clock the operation. If, however, the post-trigger event has occurred, the board continues to acquire post-trigger data using the internal retrigger clock to clock the operation.

The about-trigger operation stops when the specified number of post-trigger samples has been acquired or when you stop the operation. Refer to page 18 for more information on internally-retriggered scan mode.

Figure 6 illustrates continuous about-trigger mode using a channel-gain list of two entries: channel 0 and channel 1. In this example, pre-trigger analog input data is acquired continuously on each clock pulse of the A/D sample clock until the post-trigger event occurs. When the post-trigger event occurs, post-trigger analog input data is acquired continuously on each clock pulse of the A/D sample clock.

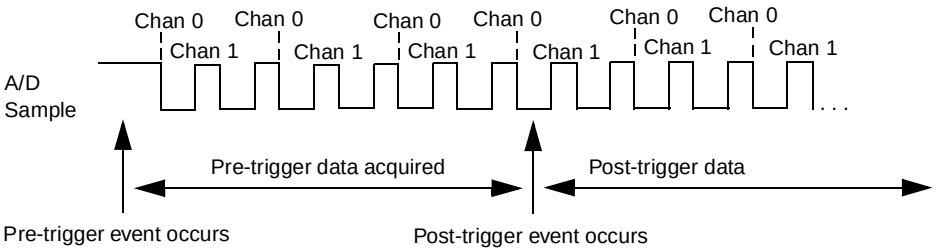


Figure 6: Continuous About-Trigger Mode

Figure 7 illustrates the same example using internally-retriggered scan mode. The multiscan count is 2, indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, pre-trigger analog input data is acquired on each clock pulse of the A/D sample clock for two scans; then, the board waits for the internal retrigger event. When the internal retrigger occurs, the board begins acquiring pre-trigger data until the post-trigger event occurs. Then, the board finishes scanning the channel-gain list the specified number of times, acquiring the data as post-trigger samples. On all subsequent internal retriggers, post-trigger data is acquired.

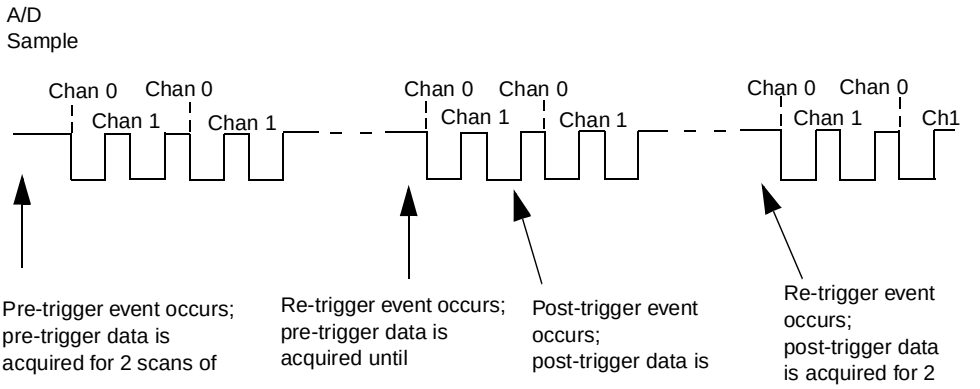


Figure 7: Continuous About-Trigger Mode with Triggered Scan

Data Format

DT300 Series boards use offset binary data encoding to represent unipolar and bipolar signals. Using software, specify the data encoding as binary.

In software, the analog input value is returned as a code. To convert the code to voltage, use the following formulas:

$$LSB = \frac{FSR}{2^N}$$

$$Vout = Code * LSB + offset$$

where,

- *LSB* is the least significant bit.
- *FSR* is the full-scale range. For the DT300 Series, the full-scale range is 10 for the unipolar range or 20 for the bipolar range.

Note: DT321 and DT322 boards support bipolar signals only.

- *N* is the number of bits of the A / D converter. For the DT301, DT302, DT303, and DT304 boards, *N* is 12. For the DT321 and DT322 boards, *N* is 16.
- *Vout* is the analog voltage.
- *Code* is the raw count used by the software to represent the voltage.
- *Offset* is the actual minus full-scale value. Theoretically, the minus full-scale value is 0.0 V for the unipolar input range and –10 V for the bipolar input range. However, the actual minus full-scale value may be slightly different than these values, such as 0.01 V and / or –9.99 V. For greatest accuracy, use the actual minus full-scale value when converting codes to voltage.

For example, assume that you are using a DT301 board with a unipolar input range. The actual minus full-scale value is 0.01 V. If the software returns a code of 2010 for the analog input operation, determine the analog input voltage as follows:

$$\text{LSB} = \frac{10}{4096} = 0.002441 \text{ V}$$

Vout = 2010 * 0.002441 + 0.01 V

Vout = 4.916 V

Similarly, assume that you are using a DT322 board with a bipolar input range. The actual minus full-scale value is –9.98 V. If the software returns a code of 2010 for the analog input operation, determine the analog input voltage as follows:

$$\text{LSB} = \frac{20}{65536} = 0.000305 \text{ V}$$

Vout = 2010 * 0.000305 + –9.98 V

Vout = –9.367 V

For the DT301, DT302, DT303, and DT304 boards, the board outputs FFFh (plus full-scale) for above-range signals and 000h (minus full-scale) for below-range signals. For the 16-bit resolution DT321 and DT322 boards, the board outputs FFFFh (plus full-scale) for above-range signals and 0000h (minus full-scale) for below-range signals.

Data Transfer

The board packs two input samples (an even and an odd sample) into each transfer to the host computer. Samples corresponding to entries 0, 2, 4, and so on, in the channel-gain list are considered even samples; samples corresponding to entries 1, 3, 5, and so on, in the channel-gain list are considered odd samples.

Using flags internally, the board determines whether the acquired samples are pre-trigger or post-trigger samples. These flags are not transferred to the host computer. The host computer can read the register on the board to determine where the post-trigger data starts. Note that the host computer cannot read data directly from the board; the data must be transferred to the host computer.

Using PCI bus mastering, the board transfers the analog input data to a 256 KB circular buffer in the host computer; this buffer is dedicated to the hardware. Therefore, unlike ISA and EISA boards, the DT300 Series board requires no DMA resources. The board treats each buffer as two consecutive 128 KB blocks of memory.

Note: When you stop an analog input operation, a final block of two samples is transferred even if only one sample is required. The host software ignores the extra sample.

The DT300 Series Device Driver accesses the hardware circular buffer to fill user buffers that you allocate in software. It is recommended that you allocate a minimum of three buffers for analog input operations, specifying a buffer wrap mode of either none (for gap-free data) or multiple, in software. The buffer wrap modes are defined as follows:

- If the wrap mode is none, data is written to the allocated buffers until no more empty buffers are available; at that point, the operation stops.
- If wrap mode is multiple, data is written to the allocated multiple buffers continuously; when no more empty buffers are available, the board overwrites the data in the filled buffers starting with the first location of the first buffer. This process continues indefinitely until you stop it.
- If wrap mode is single (usually not recommended for analog input operations), data is written to a single buffer continuously; when the buffer is filled, the board overwrites the data in the buffer starting with the first location of the buffer. This process continues indefinitely until you stop it.

Error Conditions

The DT300 Series board can report the following analog input error conditions to the host computer:

- **A/D Over Sample** – Indicates that the A/D sample clock rate is too fast. This error is reported if a new A/D sample clock pulse occurs while the ADC is busy performing a conversion from the previous A/D sample clock pulse. The host computer can clear this error. To avoid this error, use a slower sampling rate.
- **Input FIFO Overflow** – Indicates that the analog input data is not being transferred fast enough from the Input FIFO across the PCI bus to the host computer. This error is reported when the Input FIFO becomes full; the board cannot get access to the PCI bus fast enough. The host computer can clear this error, but the error will continue to be generated if the Input FIFO is still full. To avoid this error, close other applications that may be running while you are acquiring data. If this has no effect, try using a computer with a faster processor or reduce the sampling rate.
- **Host Block Overflow** – Indicates that the host computer is not handling data from the board fast enough. This error is reported if the board completes the transfer of a block of input data to the circular buffer in the host computer before the host computer has finished reading the last block of data. The host computer can clear this error. To avoid this error, ensure that you allocated at least three buffers at least as large as the sampling rate; for example, if you are using a sampling rate of 100 kSamples/s (100 kHz), specify a buffer size of 100,000 samples).

If any of these error conditions occurs, the board stops acquiring and transferring data to the host computer.

Note: DT-Open Layers reports any of these errors as an overrun message. In Windows NT 4.0, you can determine which of these errors generated the overrun message using the Event Viewer.

Analog Output Features

An analog output (D/A) subsystem is provided on the DT302, DT304, and DT322 boards only. This section describes the following features of the D/A subsystem:

- Output resolution,
- Analog output channels,
- Output ranges and gains,
- Conversion modes,
- Data formats and transfer, and
- Error conditions.

Output Resolution

Table 6 lists the output resolutions supported by the DT302, DT304, and DT322 boards. The resolution is fixed for each board type; therefore, it cannot be programmed in software.

Table 6: Supported Analog Output Resolutions

Board Type	Supported Resolution
DT302	12 bits
DT304	12 bits
DT322	16 bits

Analog Output Channels

The DT302, DT304, and DT322 boards support two serial, multiplying, DC-level analog output channels (DAC0 and DAC1). Refer to the *DT300 Series Getting Started Manual* for information on how to wire analog output signals to the board using the screw terminal panel. You configure the channel type as differential through software.

Within each DAC, the digital data is double-buffered to prevent spurious outputs, then output as an analog signal. Both DACs power up to a value of 0 V ±10 mV. Resetting the board does not clear the values in the DACs.

The DT300 Series board can output data from a single analog output channel only. Specify the channel for a single-value analog output operation using software; refer to "Conversion Modes," on this page for more information on single-value operations.

Output Ranges and Gains

For the DT302 and DT304 board, you can specify one of the following ranges for each DAC using software: ±10 V, 0 to 10 V, ±5 V, or 0 to 5 V. For the DT322 board, the range is fixed at ±10 V.

In software, specify a gain of 1 for analog output operations.

Conversion Modes

DT302, DT304, and DT322 boards can perform single-value operations only. Use software to specify the range, gain, and analog output channel (among other parameters), then output the data from the specified channel. You cannot specify a clock source, trigger source, or buffer.

Single-value operations stop automatically when finished; you cannot stop a single-value operation.

Data Format

Data from the host computer must use offset binary data encoding for analog output signals. Using software, specify the data encoding as binary.

In software, you need to supply a code that corresponds to the analog output value you want the board to output. To convert a voltage to a code, use the following formulas:

$$LSB = \frac{FSR}{2^N}$$

$$Code = \frac{Vout - offset}{LSB}$$

where,

- *LSB* is the least significant bit.
- *FSR* is the full-scale range. For the DT300 Series, the full-scale analog output range is 5 for the unipolar range of 0 to 5 V; 10 for the unipolar range of 0 to 10 V or the bipolar output range of ±5 V; or 20 for the bipolar range or ±10V.
- *N* is the number of bits of the D/A converter. For the DT302 and DT304 boards, *N* is 12. For the DT322 board, *N* is 16.
- *Code* is the raw count used by the software to represent the voltage.
- *Vout* is the analog voltage.
- *Offset* is the minus full-scale value. The minus full-scale value is 0.0 V for the unipolar range and either –5 V for the ±5 V range or –10 V for the ±10 V range.

For example, assume that you are using a DT302 board with a unipolar output range of 0 to 5 V. The minus full-scale value is 0 V. If you want to output a voltage of 4.7V, determine the code value as follows:

$$\text{LSB} = \frac{5}{4096} = 0.001221 \text{ V}$$

$$\text{Code} = \frac{4.7 \text{ V} - 0 \text{ V}}{0.001221 \text{ V}}$$

Code = 3849 = 0F09h

Similarly, assume that you are using a DT322 board with a bipolar output range of ±10 V. The minus full-scale value is –10 V. If you want to output a voltage of 4.7V, determine the code value as follows:

$$\text{LSB} = \frac{20}{65536} = 0.000305 \text{ V}$$

$$\text{Code} = \frac{4.7 \text{ V} - (-10 \text{ V})}{0.000305 \text{ V}}$$

Code = 48196 = BC44h

Digital I/O Features

This section describes the following features of the digital I/O subsystem:

- Digital I/O lines,
- Digital I/O resolution, and
- Digital I/O operation modes.

Digital I/O Lines

DT300 Series boards support 23 digital I/O lines through the digital input (DIN) and output (DOUT) subsystems; DIN and DOUT subsystems use the same digital I/O lines. These lines are divided into the following ports:

- Port A, lines 0 to 7,
- Port B, lines 0 to 7, and
- Port C, lines 0 to 6.

You can use each port for either input or output; all lines within a port have the same configuration. For example, if you use Port A as an input port, lines 0 to 7 of Port A are configured as inputs. Likewise, if you use Port C as an output port, lines 0 to 6 of Port C are configured as outputs.

For fast, clocked digital input operations, you can enter the digital I/O lines from Ports A and B as a channel in the analog input channel list; refer to page 11 for more information.

By default, the digital I/O lines power up as digital inputs. On power up or reset, no digital data is output from the board.

Digital I/O Resolution

For Ports A and B, you can specify the number of lines to read or write by specifying the resolution in software. If you specify a resolution of 8, element 0 (the first subsystem) corresponds to the Port A, lines 0 to 7; element 1 (the second subsystem) corresponds to Port B, lines 0 to 7; and element 2 (the third subsystem) corresponds to Port C, lines 0 to 6.

If you specify a resolution of 16, element 0 corresponds to Ports A and B, lines 0 to 15; element 1 also corresponds to Ports A and B, lines 0 to 15; and element 2 corresponds to Port C, lines 0 to 6.

Note: When the resolution is 16, digital I/O lines 0 to 7 of Port B are represented as bits 8 to 15 of the digital value; do not use element 0 and element 1 at the same time.

The resolution of Port C is fixed at 7; Port C cannot be combined with Port A or B.

Digital I/O Operation Modes

The DT300 Series board supports the following digital I/O operation modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. You use software to specify the digital I/O lines and a gain of 1 (the gain is ignored). Data is then read from or written to the digital I/O lines. For a single-value operation, you cannot specify a clock or trigger source.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous digital input** takes full advantage of the capabilities of the DT300 Series board. In this mode, enter all 16 digital input lines of Ports A and B as channel 16 of the analog input channel-gain list; program this mode through the A/D subsystem. Using this mode, you can specify a clock source, scan mode, trigger source, buffer, and buffer wrap mode for the digital input operation. Refer to page 11 for more information on specifying digital input lines for a continuous digital input operation.

Counter/Timer Features

The counter / timer circuitry on the board provides the clocking circuitry used by the A / D subsystem as well as several user counter / timer features. This section describes the following user counter / timer features:

- Counter / timer channels,
- C / T clock sources,
- Gate types,
- Pulse types and duty cycles, and
- Counter / timer operation modes.

Counter/Timer Channels

The DT300 Series board supports four user 16-bit counter / timer channels (called counters); counters are numbered 0, 1, 2, and 3.

Each counter accepts a clock input signal and gate input signal and outputs a clock output signal (also called a pulse output signal), as shown in Figure 8.

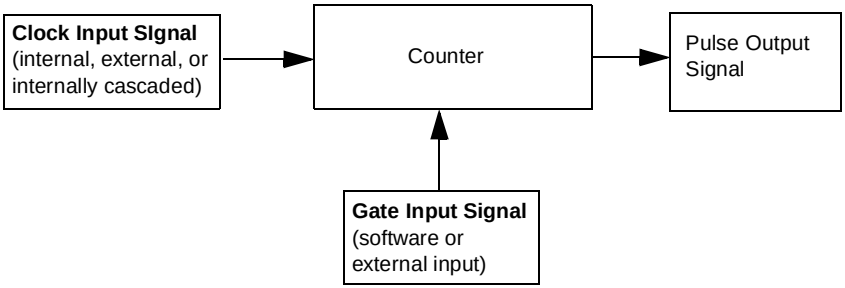


Figure 8: Counter/Timer Channel

Each counter corresponds to a counter/timer (C/T) subsystem. To specify the counter to use in software, specify the appropriate C/T subsystem. For example, counter 0 corresponds to C/T subsystem element 0; counter 3 corresponds to C/T subsystem element 3.

Using software, you can internally route the clock output signal from one user counter to the clock input signal of the next user counter to internally cascade the counters. In this way, you can create a 32-bit counter without externally connecting two counters together.

C/T Clock Sources

The following clock sources are available for the user counters:

- Internal C/T clock,
- External C/T clock, and
- Internally cascaded clock.

Refer to the following subsections for more information on these clock sources.

Internal C/T Clock

The internal C/T clock uses a 20 MHz time base. Counter/timer operations start on the rising edge of the clock input signal.

Through software, specify the clock source as internal and the frequency at which to pace the counter/timer operation (this is the frequency of the clock output signal). The maximum frequency that you can specify for the clock output signal is 10 MHz. For a 16-bit counter, the minimum frequency that you can specify for the clock output signal is 305.17 Hz. For a 32-bit cascaded counter, the minimum frequency that you can specify for the clock output signal is 0.00465 Hz, which corresponds to a rate of once every 215 seconds.

External C/T Clock

The external C/T clock is useful when you want to pace counter/timer operations at rates not available with the internal C/T clock or if you want to pace at uneven intervals. The rising edge of the external C/T clock input signal is the active edge.

Using software, specify the clock source as external and the clock divider used to determine the frequency at which to pace the operation (this is the frequency of the clock output signal). The minimum clock divider that you can specify is 2.0; the maximum clock divider that you can specify is 65535. For example, if you supply an external C/T clock with a frequency of 5 MHz and specify a clock divider of 5, the resulting frequency of the external C/T clock output signal is 1 MHz. The resulting frequency of the external C/T clock output signal must not exceed 2.5 MHz.

Connect the external C/T clock source to the board through the STP300 screw terminal panel as follows:

- For Counter 0, connect the external C/T clock signal to screw terminal TB26 (pin 41 of connector J1),
- For Counter 1, connect the external C/T clock signal to screw terminal TB30 (pin 7 of connector J1),
- For Counter 2, connect the external C/T clock signal to screw terminal TB34 (pin 36 of connector J1), and
- For Counter 3, connect the external C/T clock signal to screw terminal TB38 (pin 2 of connector J1).

Internally Cascaded Clock

The DT300 Series board supports internal cascading on counters 0 and 1, 1 and 2, and 2 and 3. Cascading counters internally is an effective way to create a 32-bit counter without externally connecting two counters together.

Using software, specify internal cascade mode, then specify the clock input and gate input for the first counter in the cascaded pair. The clock output signal from first counter is the clock input signal of the second counter. For example, if counters 1 and 2 are cascaded, specify the clock input and gate input for counter 1.

The rising edge of the clock input signal is active.

Gate Types

The active edge or level of the gate input to the counter enables counter / timer operations. The operation starts when the clock input signal is received. The DT300 Series board provides the following gate input types:

- **None** – A software command enables any specified counter / timer operation immediately after execution. This gate type is useful for all counter / timer modes.
- **Logic-low level external gate input** – Enables a counter / timer operation when the external gate signal is low, and disables the counter / timer operation when the external gate signal is high. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 49 for more information on these modes.
- **Logic-high level external gate input** – Enables a counter / timer operation when the external gate signal is high, and disables a counter / timer operation when the external gate signal is low. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 49 for more information on these modes.
- **Falling edge external gate input** – Triggers a counter / timer operation on the transition from the high level to the low level (falling edge). In software, this is called a low edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 49 for more information on these modes.

- **Rising edge external gate input** – Triggers a counter/timer operation on the transition from the low level to the high level (rising edge). In software, this is called a high-edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 49 for more information on these modes.

Specify the gate type in software. Connect an external gate input to the board through the STP300 screw terminal panel as follows:

- For Counter 0, connect the external gate signal to screw terminal TB28 (pin 39 of connector J1),
- For Counter 1, connect the external gate signal to screw terminal TB32 (pin 5 of connector J1),
- For Counter 2, connect the external gate signal to screw terminal TB36 (pin 38 of connector J1), and
- For Counter 3, connect the external gate signal to screw terminal TB40 (pin 4 of connector J1).

Pulse Outputs

The DT300 Series boards provide the following C/T pulse output signals:

- For Counter 0, the C/T output signal is screw terminal TB27 (pin 40 of connector J1),
- For Counter 1, the C/T output signal is screw terminal TB31 (pin 6 of connector J1),
- For Counter 2, the C/T output signal is screw terminal TB35 (pin 37 of connector J1), and
- For Counter 3, the external C/T output signal is screw terminal TB39 (pin 3 of connector J1).

The DT300 Series board supports the following pulse output types on the clock output signal:

- **High-to-low transitions** – The low portion of the total pulse output period is the active portion of the counter / timer clock output signal.
- **Low-to-high transitions** – The high portion of the total pulse output period is the active portion of the counter / timer pulse output signal.

Using software, you can specify the duty cycle of the pulse. The duty cycle (or pulse width) indicates the percentage of the total pulse output period that is active. A duty cycle of 50, then, indicates that half of the total pulse is low and half of the total pulse output is high. Figure 9 illustrates a low-to-high pulse with a duty cycle of approximately 30%.

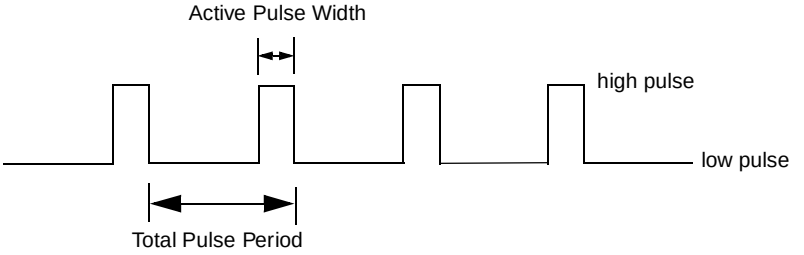


Figure 9: Example of a Low-to-High Pulse Output Type

Counter/Timer Operation Modes

The DT300 Series board supports the following counter/timer operation modes:

- Event counting,
- Frequency measurement,
- Rate generation,
- One-shot, and
- Repetitive one-shot.

Refer to the following subsections for more information on these operation modes.

Event Counting

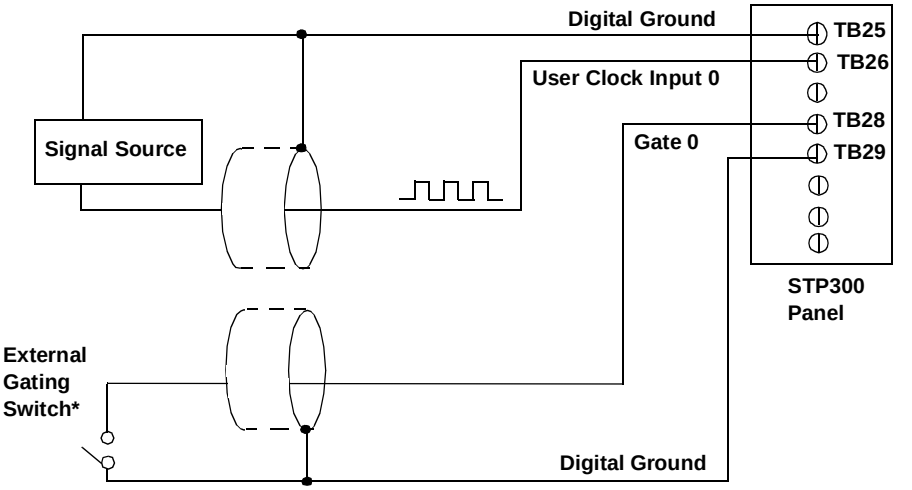
Use event counting mode to count events from the counter's associated clock input source.

If you are using one counter, the board can count a maximum of 65,536 events before the counter rolls over to 0 and starts counting again. If you are using a cascaded 32-bit counter, the board can count a maximum of 4,294,967,296 events before the counter rolls over to 0 and starts counting again.

In event counting mode, use an external C/T clock source; refer to page 45 for more information on the external C/T clock source.

Using software, specify the counter/timer mode as event counting (count), the clock source as external, and the gate type that enables the operation. Refer to page 46 for more information on gate types.

Ensure that the signals are wired appropriately. Figure 10 shows one example of connecting an event counting application to the STP300 screw terminal panel using user counter 0. In this example, rising clock edges are counted while the gate is active.



***An internal 22 kΩ pull-up resistor to +5 V is used.**

Figure 10: Connecting Event Counting Signals (Shown for Clock Input 0 and External Gate 0)

Figure 11 shows an example of performing an event counting operation. In this example, the gate type is low level.

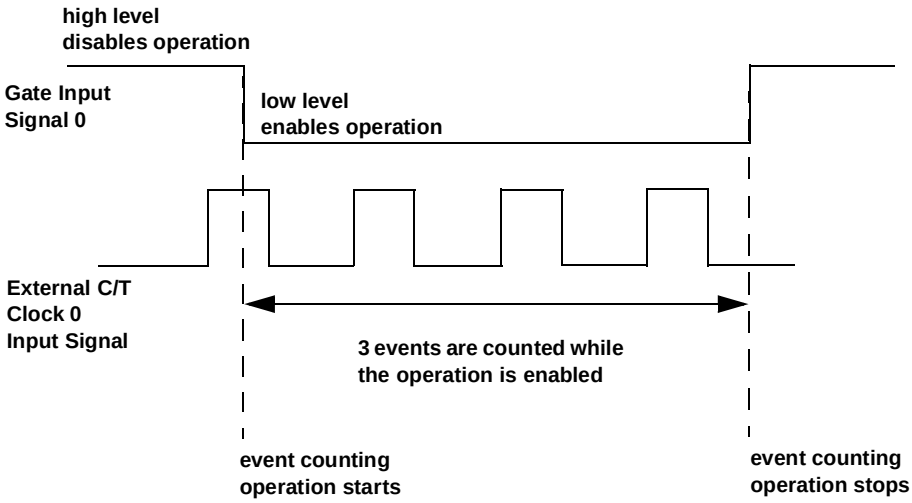


Figure 11: Example of Event Counting

Frequency Measurement

Use frequency measurement mode to measure the frequency of the signal from counter's associated clock input source over a specified duration. In this mode, use an external C/T clock source; refer to page 45 for more information on the external C/T clock source.

One way to perform a frequency measurement is to use the same wiring as an event counting application that does not use an external gate signal, as shown in Figure 12.

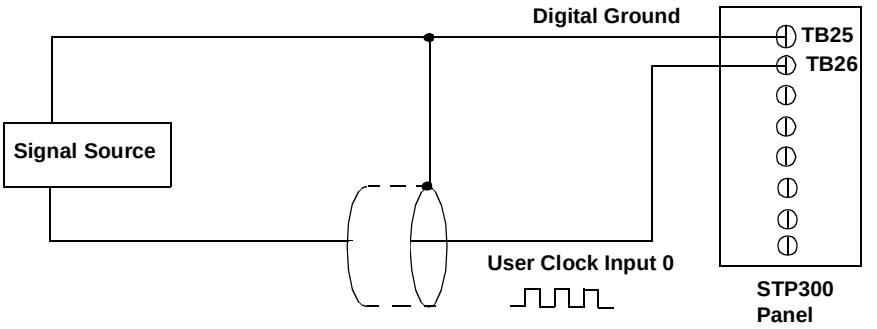


Figure 12: Connecting Frequency Measurement Signals without an External Gate Input (Shown for Clock Input 0)

In this configuration, use software to specify the counter/timer mode as frequency measurement or event counting, and the duration of the Windows timer over which to measure the frequency. (The Windows timer uses a resolution of 1 ms.) In this configuration, frequency is determined using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Duration of the Windows Timer}}$$

If you need more accuracy than the Windows timer provides, you can connect a pulse of a known duration (such as a one-shot output of another user counter) to the external gate input, as shown in Figure 13.

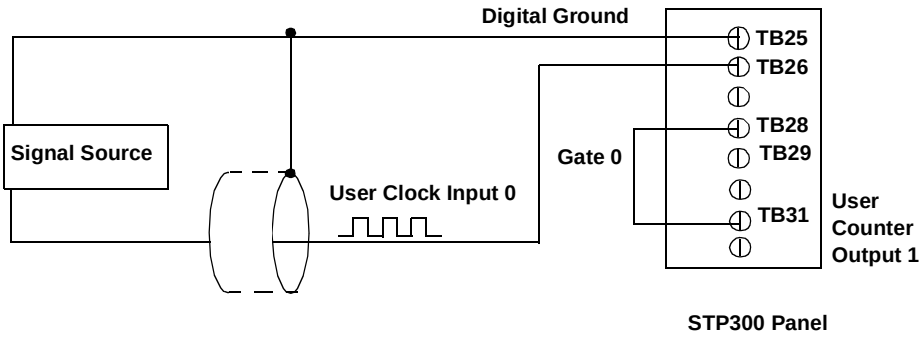


Figure 13: Connecting Frequency Measurement Signals (Shown for Clock Input 0 and External Gate 0)

In this configuration, use software to set up the counter / timers as follows:

1. Set up one of the counter / timers for one-shot mode, specifying the clock source, clock frequency, gate type, type of output pulse (high or low), and pulse width.
2. Set up the counter / timer that will measure the frequency for event counting mode, specifying the clock source to count, and the gate type (this should match the pulse output type of the counter / timer set up for one-shot mode);
3. Start both counters (events are not counted until the active period of the one-shot pulse is generated);
4. Read the number of events counted (allow enough time to ensure that the active period of the one-shot occurred and that events have been counted).
5. Determine the measurement period using the following equation:

$$\text{Measurement period} = \frac{1}{\text{Clock Frequency}} * \text{Active Pulse Width}$$

6. Determine the frequency of the clock input signal using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Measurement Period}}$$

Figure 14 shows an example of performing a frequency measurement operation. In this example, three events are counted during a duration of 300 ms. The frequency, then, is 10 Hz, since 10 Hz = 3/(.3 s).

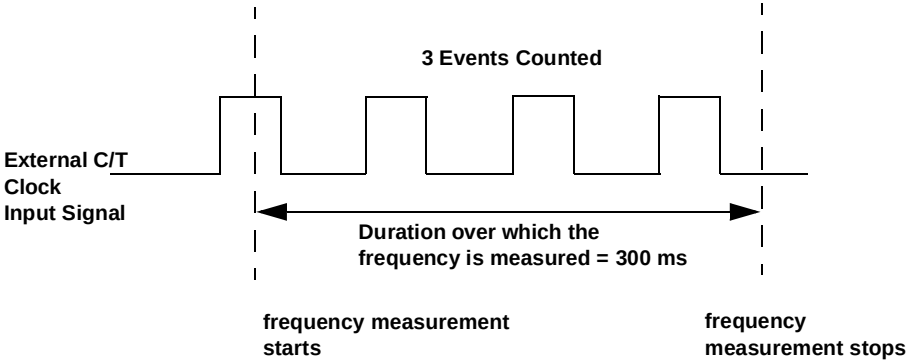


Figure 14: Example of Frequency Measurement

Rate Generation

Use rate generation mode to generate a continuous pulse output signal from the counter; this mode is sometimes referred to as continuous pulse output or pulse train output. You can use this pulse output signal as an external clock to pace other operations, such as analog input or other counter/timer operations.

While the pulse output operation is enabled (determined by the gate input signal), the counter outputs a pulse of the specified type and frequency continuously. As soon as the operation is disabled, rate generation stops.

The period of the output pulse is determined by the clock input signal and external clock divider. If you are using one counter (not cascaded), you can output pulses using a maximum frequency of 10 MHz. In rate generation mode, either the internal or external C/T clock input source is appropriate depending on your application; refer to page 44 for more information on the C/T clock source.

Using software, specify the counter/timer mode as rate generation (rate), the C/T clock source as either internal or external, the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, and the gate type that enables the operation. Refer to page 47 for more information on the pulse output types; refer to page 46 for more information on gate types.

Ensure that the signals are wired appropriately. Figure 15 shows one example of connecting a pulse output operation to the STP300 screw terminal panel using user counter 0. In this example, a software gate type is used.

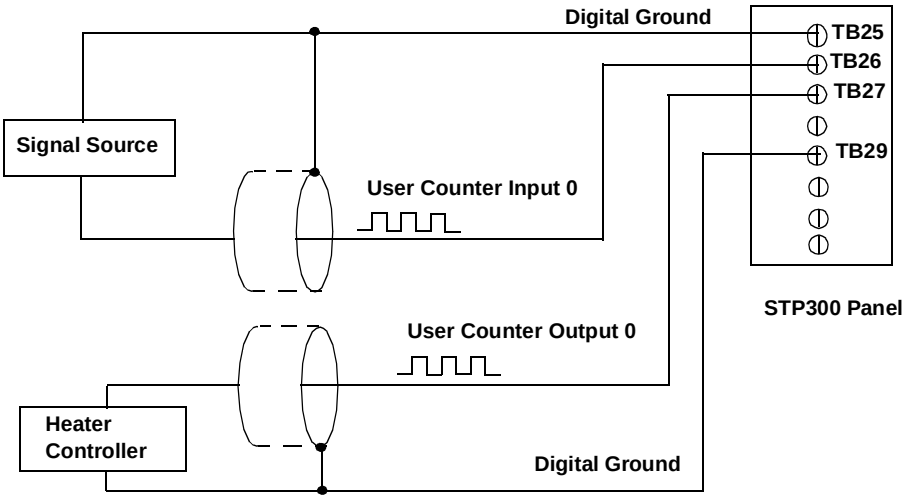


Figure 15: Connecting Rate Generation SIgnals (Shown for Counter 0; a Software Gate Is Used)

Figure 16 shows an example of performing an enabled rate generation operation using an external C/T clock source with an input frequency of 4 kHz, a clock divider of 4, a low-to-high pulse type, and a duty cycle of 75%. (The gate type does not matter for this example.) A 1 kHz square wave is the generated output. Figure 17 shows the same example using a duty cycle of 25%.

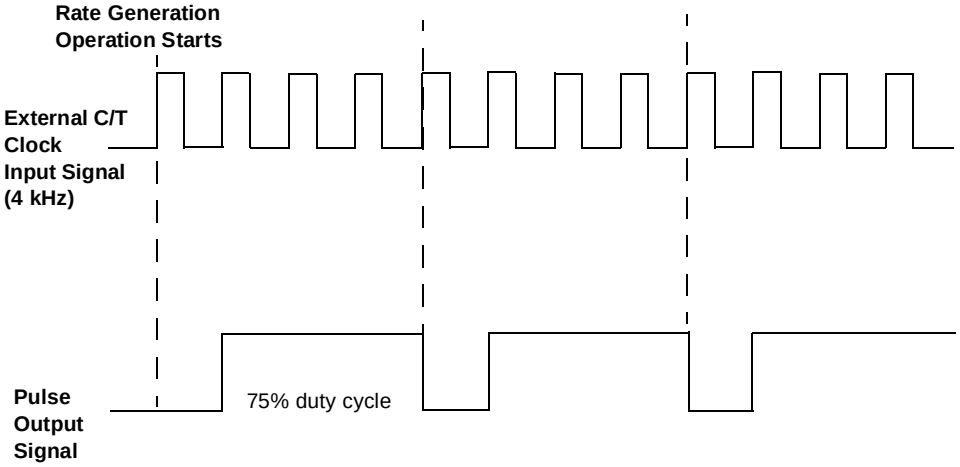


Figure 16: Example of Rate Generation Mode with a 75% Duty Cycle

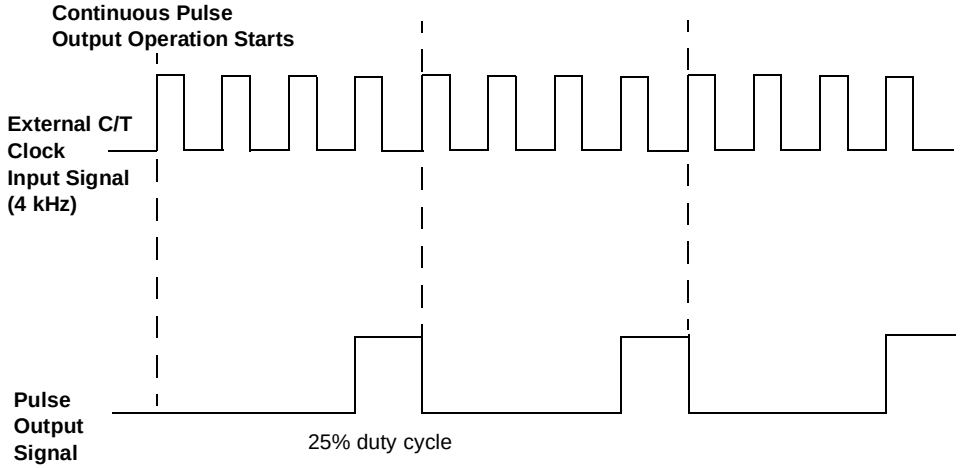


Figure 17: Example of Rate Generation Mode with a 25% Duty Cycle

One-Shot

Use one-shot mode to generate a single pulse output signal from the counter when the operation is triggered (determined by the gate input signal). You can use this pulse output signal as an external digital (TTL) trigger to start other operations, such as analog input or an external instrument.

When the one-shot operation is triggered and a single pulse is output; then, the one-shot operation stops. All subsequent clock input signals and gate input signals are ignored.

The period of the output pulse is determined by the clock input signal. In one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 44 for more information on the internal C/T clock source.

Using software, specify the counter/timer mode as one-shot, the clock source as internal, the polarity of the output pulse (high-to-low transition or low-to-high transition), the duty cycle of the output pulse, and the gate type to trigger the operation. Refer to page 47 for more information on pulse output types. Refer to page 46 for more information on gate types.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

Ensure that the signals are wired appropriately. Figure 15 shows one example of connecting a pulse output operation to the STP300 screw terminal panel using user counter 0.

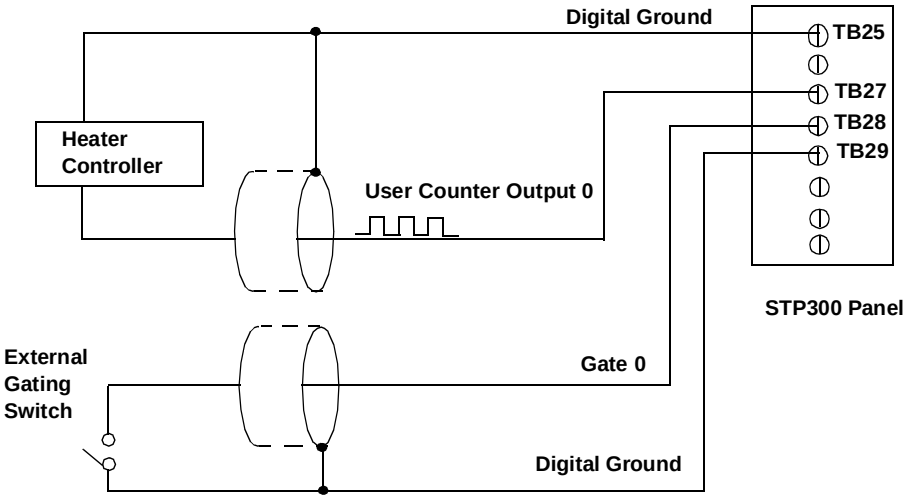


Figure 18: Connecting One-Shot Signals (Shown for Counter Output 0 and Gate 0)

Figure 19 shows an example of performing a one-shot operation using an external gate input (rising edge), a clock output frequency of 1 kHz (pulse period of 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 20 shows the same example using a duty cycle of 50%

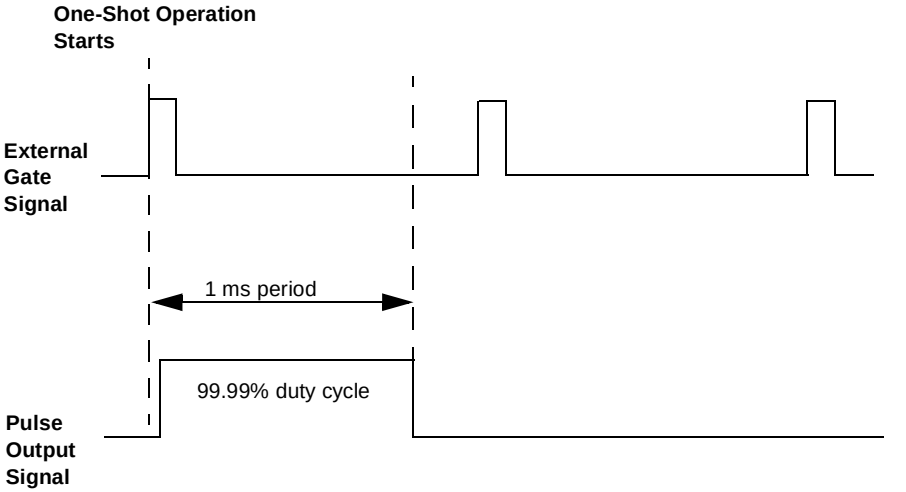


Figure 19: Example of One-Shot Mode Using a 99.99% Duty Cycle

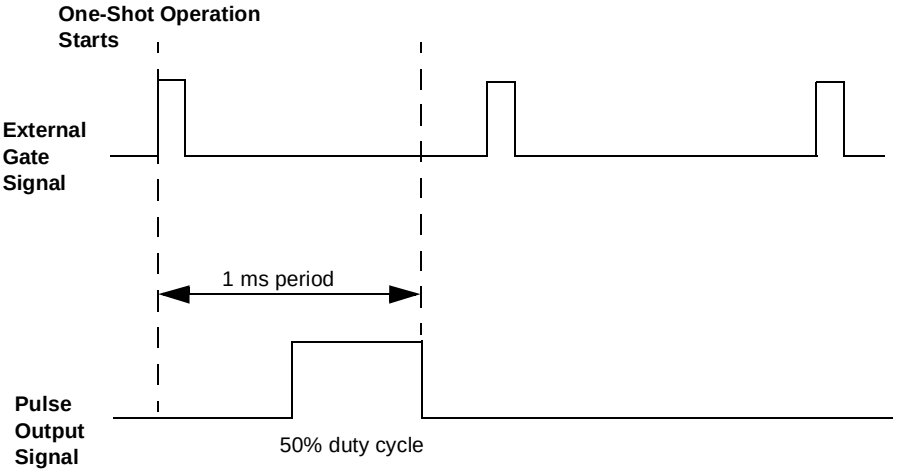


Figure 20: Example of One-Shot Mode Using a 50% Duty Cycle

Repetitive One-Shot

Use repetitive one-shot mode to generate a pulse output signal each time the board detects a trigger (determined by the gate input signal). You can use this mode to clean up a poor clock input signal by changing its pulse width, then outputting it.

When the one-shot operation is triggered (determined by the gate input signal), a pulse is output. When the board detects the next trigger, another pulse is output. This operation continues until you stop the operation.

The period of the output pulse is determined by the clock input signal. In repetitive one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 44 for more information on the internal C/T clock source.

Using software, specify the counter/timer mode as repetitive one-shot (oneshot-rpt for SDK users), the clock source as internal, the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, and the gate type to trigger the operation. Refer to page 47 for more information on pulse output types; refer to page 46 for more information on gate types.

Note: In the case of a repetitive one-shot operation, use a duty cycle as close to 100% as possible to output each pulse immediately after the trigger occurs. Using a duty cycle closer to 0% acts as a pulse output delay.

Ensure that the signals are wired appropriately. Refer to Figure 18 on page 59 for a wiring example.

Note: Triggers that occur while the pulse is being output are not detected by the board.

Figure 21 shows an example of a repetitive one-shot operation using an external gate (rising edge); a clock output frequency of 1 kHz (pulse period of 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 22 shows the same example using a duty cycle of 50%.

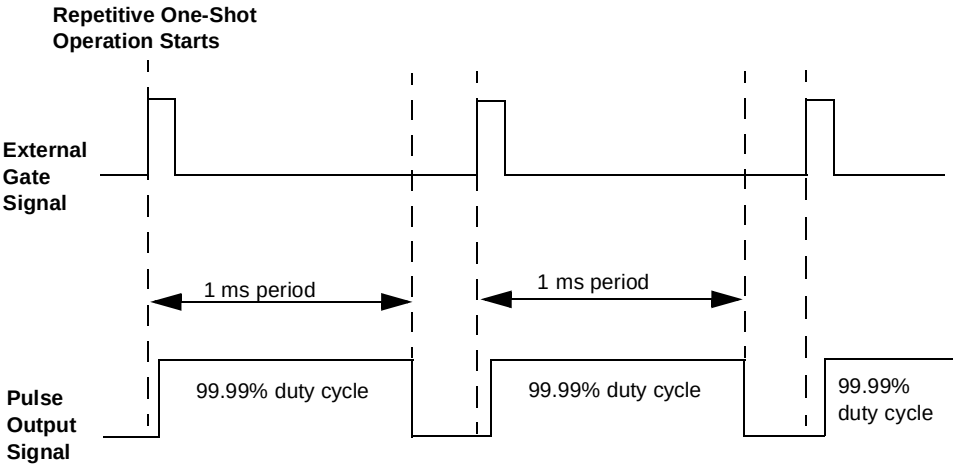


Figure 21: Example of Repetitive One-Shot Mode Using a 99.99% Duty Cycle

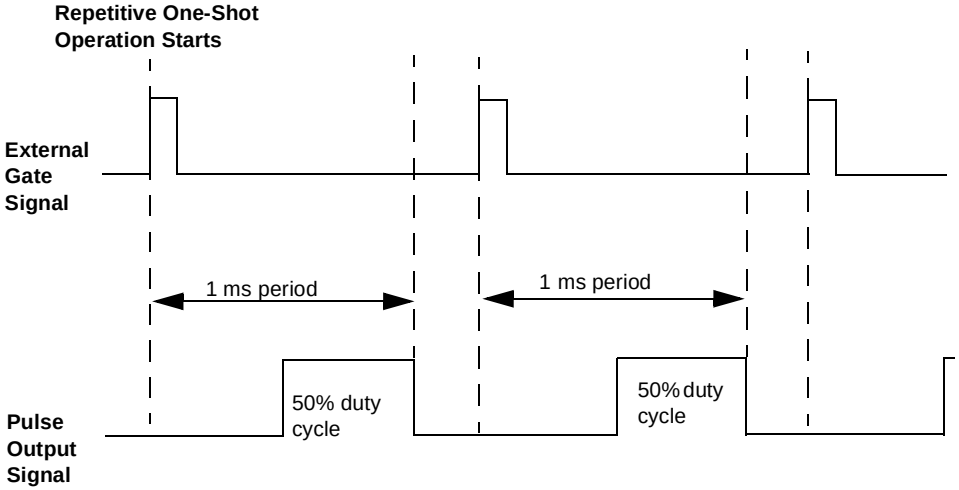


Figure 22: Example of Repetitive One-Shot Mode Using a 50% Duty Cycle

3

Supported Device Driver Capabilities

The DT300 Series Device Driver provides support for A/D, D/A, DIN, DOUT, and C/T subsystems. For information on how to install the device driver, refer to the *DT300 Series Getting Started Manual.*

Table 1 summarizes the board features available for use with the DataAcq SDK. The DataAcq SDK provides functions that return support information for specified subsystem capabilities at runtime.

The first row in the table lists the subsystem types. The first column in the table lists all possible subsystem capabilities. A description of each capability is followed by the parameter used to describe that capability in the DataAcq SDK.

Note: Blank fields represent unsupported options.

The DataAcq SDK uses the functions **olDaGetSSCaps** (for those queries starting with OLSSC) and **olDaGetSSCapsEx** (for those queries starting with OLSSCE) to return the supported subsystem capabilities for a device.

For more information, refer to the description of these functions in the DataAcq SDK online help. See the *DataAcq User's Manual* for information on opening this help file.

Table 7: DT300 Series Supported Options

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Data Flow Mode	Single-Value Operation Support OLSSC_SUP_SINGLEVALUE	Yes	Yes	Yes	Yes		
	Continuous Operation Support OLSSC_SUP_CONTINUOUS	Yes		Yes[c]			Yes
	Continuous Operation until Trigger Event Support OLSSC_SUP_CONTINUOUS_PRETRIG	Yes					
	Continuous Operation before and after Trigger Event OLSSC_SUP_CONTINUOUS_ABOUTTRIG	Yes					
	DT-Connect Support OLSSC_SUP_DTCONNECT						
	Continuous DT-Connect Support OLSSC_SUP_DTCONNECT_CONTINUOUS						
	Burst DT-Connect Support OLSSC_SUP_DTCONNECT_BURST						
Sim. Oper.	Simultaneous Start List Support OLSSC_SUP_SIMULTANEOUS_START						
Pause Oper.	Pause Operation Support OLSSC_SUP_PAUSE						
Wind. Mess.	Asynchronous Operation Support OLSSC_SUP_POSTMESSAGE	Yes					
Buffering	Buffer Support OLSSC_SUP_BUFFERING	Yes					
	Single Buffer Wrap Mode Support OLSSC_SUP_WRPSINGLE	Yes					

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Buffering (cont.)	Multiple Buffer Wrap Mode Support OLSSC_SUP_WRPMULTIPLE	Yes					
	Inprocess Buffer Flush Support OLSSC_SUP_INPROCESSFLUSH	Yes					
DMA	Number of DMA Channels OLSSC_NUMDMACHANS	0	0	0	0		0
	Supports Gap Free Data with No DMA OLSSC_SUP_GAPFREE_NODMA	Yes					
	Supports Gap Free Data with Single DMA OLSSC_SUP_GAPFREE_SINGLEDMA						
	Supports Gap Free Data with Dual DMA OLSSC_SUP_GAPFREE_DUALDMA						
Triggered Scan Mode	Triggered Scan Support OLSSC_SUP_TRIGSCAN	Yes					
	Maximum Number of CGL Scans per Trigger OLSSC_MAXMULTISCAN	256[d]	0	0	0		0
	Supports Scan perTrigger Event Triggered Scan OLSSC_SUP_RETRIGGER_SCAN_PER_TRIGGER	Yes					
	Supports Internal Retriggered Triggered Scan OLSSC_SUP_RETRIGGER_INTERNAL	Yes					
	Extra Retrigger Support OLSSC_SUP_RETRIGGER_EXTRA	Yes					

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Triggered Scan Mode (cont.)	Maximum Retrigger Frequency OLSSCE_MAXRETRIGGER	155 kHz, 219 kHz, or 165 kHz[e]	0	0	0		0
	Minimum Retrigger Frequency OLSSCE_MINRETRIGGER	1.2 Hz[f]	0	0	0		0
Channel-Gain List	Maximum Channel Gain List Depth OLSSC_CGLDEPTH	1024	1	0[c]	0[c]		0
	Sequential Channel Gain List Support OLSSC_SUP_SEQUENTIAL_CGL	Yes					
	Zero Start Sequential Channel Gain List Support OLSSC_SUP_ZEROSEQUENTIAL_CGL	Yes					
	Random Channel-Gain List Support OLSSC_SUP_RANDOM_CGL	Yes					
	Simultaneous Sample and Hold Support OLSSC_SUP_SIMULTANEOUS_SH						
	Channel List Inhibit Support OLSSC_SUP_CHANNELLIST_INHIBIT	Yes					
Gain	Programmable Gain Support OLSSC_SUP_PROGRAMGAIN	Yes					
	Number of Gains OLSSC_NUMGAINS	4	1	1	1		0
	AutoRanging Support OLSSC_SINGLEVALUE_AUTORANGE						

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Synchronous Digital I/O	Synchronous Digital I/O Support OLSSC_SUP_SYNCHRONOUS_DIGITALIO						
	Maximum Synchronous Digital I/O Value OLSSC_MAX_DIGITALIOLIST_VALUE	0	0	0	0		0
I/O Channels	Number of Channels OLSSC_NUMCHANNELS	17[g]	2	1	1		1
	DT2896 Channel Expansion Support OLSSC_SUP_EXP2896						
	DT727 Channel Expansion OLSSC_SUP_EXP727						
Channel Type	SE Support OLSSC_SUP_SINGLEENDED	Yes					
	SE Channels OLSSC_MAXSECHANS	16	0	0	0		0
	DI Support OLSSC_SUP_DIFFERENTIAL	Yes	Yes	Yes	Yes		
	DI Channels OLSSC_MAXDICHANS	8	2	1	1		1
Filters	Filter/Channel Support OLSSC_SUP_FILTERPERCHAN						
	Number of Filters OLSSC_NUMFILTERS	1	1	1	1		0
Ranges	Number of Voltage Ranges OLSSC_NUMRANGES	2[h]	4 or 1[i]	0	0		0
	Range per Channel Support OLSSC_SUP_RANGEPERCHANNEL						

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Resolution	Software Programmable Resolution OLSSC_SUP_SWRESOLUTION			Yes[j]	Yes[j]		
	Number of Resolutions OLSSC_NUMRESOLUTIONS	1	1	2[j]	2[j]		1
Data Encoding	Binary Encoding Support OLSSC_SUP_BINARY	Yes	Yes	Yes	Yes		Yes
	Twos Complement Support OLSSC_SUP_2SCOMP						
Triggers	Software Trigger Support OLSSC_SUP_SOFTTRIG	Yes	Yes	Yes	Yes		Yes
	External Trigger Support OLSSC_SUP_EXTERNTRIG	Yes[k]					Yes
	Positive Threshold Trigger Support OLSSC_SUP_THRESHTRIGPOS						
	Negative Threshold Trigger Support OLSSC_SUP_THRESHTRIGNEG						
	Analog Event Trigger Support OLSSC_SUP_ANALOGEVENTTRIG						
	Digital Event Trigger Support OLSSC_SUP_DIGITALEVENTTRIG						
	Timer Event Trigger Support OLSSC_SUP_TIMEREVENTTRIG						
	Number of Extra Triggers OLSSC_NUMEXTRATRIGGERS	1[k]	0	0	0		0

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Clocks	Internal Clock Support OLSSC_SUP_INTCLOCK	Yes	Yes				Yes
	External Clock Support OLSSC_SUP_EXTCLOCK	Yes					Yes
	Number of Extra Clocks OLSSC_NUMEXTRACLOCKS	0	0	0	0		0
	Base Clock Frequency OLSSCE_BASECLOCK	20 MHz	0	0	0		20 MHz
	Maximum External Clock Divider OLSSCE_MAXCLOCKDIVIDER	1.0	1.0	1.0	1.0		65536
	Minimum External Clock Divider OLSSCE_MINCLOCKDIVIDER	1.0	1.0	1.0	1.0		2.0
	Maximum Throughput OLSSCE_MAX_THROUGHPUT	3 MHz[l]	1.0 Hz	0	0		10 MHz[m]
	Minimum Throughput OLSSCE_MIN_THROUGHPUT	1.2 Hz	1.0 Hz	0	0		0.005 Hz[n]
Counter/Timers	Cascading Support OLSSC_SUP_CASCADING						Yes
	Event Count Mode Support OLSC_SUP_CTMODE_COUNT						Yes
	Generate Rate Mode Support OLSSC_SUP_CTMODE_RATE						Yes
	One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT						Yes
	Repetitive One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT_RPT						Yes
	High to Low Output Pulse Support OLSSC_SUP_PLS_HIGH2LOW						Yes

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Counter/Timers (cont.)	Low to High Output Pulse Support OLSSC_SUP_PLS_LOW2HIGH						Yes
	None (internal) Gate Type Support OLSSC_SUP_GATE_NONE						Yes
	High Level Gate Type Support OLSSC_SUP_GATE_HIGH_LEVEL						Yes[o]
	Low Level Gate Type Support OLSSC_SUP_GATE_LOW_LEVEL						Yes[o]
	High Edge Gate Type Support OLSSC_SUP_GATE_HIGH_EDGE						Yes[o]
	Low Edge Gate Type Support OLSSC_SUP_GATE_LOW_EDGE						Yes[o]
	Level Change Gate Type Support OLSSC_SUP_GATE_LEVEL						
	High Level Gate Type with Input Debounce Support OLSSC_SUP_GATE_HIGH_LEVEL_DEBOUNCE						
	Low Level Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_LEVEL_DEBOUNCE						
	High Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_HIGH_EDGE_DEBOUNCE						

Table 7: DT300 Series Supported Options (cont.)

	DT300 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2**	**3[b]**	**3[b]**	**0**	**4**
Counter/Timers (cont.)	Low Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_EDGE_DEBOUNCE Level Change Gate Type with Input Debounce Support OLSSC_SUP_GATE_LEVEL_DEBOUNCE						
Interrupt	Interrupt Support OLSSC_SUP_INTERRUPT						
FIFOs	FIFO in Data Path Support OLSSC_SUP_FIFO						
Processor	Data Processing Capability OLSSC_SUP_PROCESSOR						
Software Calibration	Software Calibration Support OLSSC_SUP_SWCAL	Yes	Yes				

a. D / A subsystems are supported by the DT302, DT304, and DT322 boards only.

b. The DIN and DOUT subsystems use the same DIO lines.

c. All 16 bits of the DIO lines from Ports A and B are assigned to A / D input channel 16. While the DIN subsystem itself is incapable of continuous operation, you can perform a continuous DIN operation by specifying channel 16 in the channel-gain list of the A / D subsystem and starting the A / D subsystem.

d. The CGL depth of 1024 entries in conjunction with a multiscan count of 256 provides an effective CGL depth of up to 256K entries.

e. The maximum retrigger frequency depends on the board type. For DT301 and DT302 boards, the maximum retrigger frequency is 155 kHz. For DT303 and DT304 boards, the maximum retrigger frequency is 219 kHz. For DT321 and DT322 boards, the maximum retrigger frequency is 165 kHz. The maximum retrigger frequency is based on the number of samples per trigger, as follows:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries x \# of CGLs per trigger}}{\text{A/D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

f. The value of 1.2 Hz assumes the minimum number of samples is 1.

g. Channels 0 to 15 are provided for analog input; channel 16 reads all 16 bits from the DIN subsystem (Ports A and B). If the channel-gain list contains channel 16 only, the board can read the digital input channels at a rate of 3 MSamples/s.

h. DT301, DT302, DT303, and DT304 boards support two input ranges: ±10 V and 0 to 10 V. DT321 and DT322 boards support one input range: ±10V.

i. DT302 and DT304 boards support four output ranges: ±10 V, 0 to 10 V, ±5 V, and 0 to 5 V. DT322 boards support one output range: ±10 V.

j. When configured for 16 bits of resolution, both element 0 and element 1 use DIO bits 15 to 0 (Ports A and B are combined); however, you cannot use both elements at the same time. When configured for 8 bits of resolution, element 0 uses bits 7 to 0 (Port A) and element 1 uses bits 15 to 8 (Port B). Port C (element 2) always uses a fixed resolution of 7 and cannot be combined with Port A or Port B.

k. OL_TRG_EXTERN is the rising-edge external digital (TTL) trigger input; OL_TRG_EXTRA is the falling-edge digital external (TTL) trigger input.

l. For DT301 and DT302 boards, the maximum throughput for analog input channels is 225 kHz; for DT303 and DT304 boards, the maximum throughput for analog input channels is 400 kHz; for DT321 and DT322 boards, the maximum throughput for analog input channels is 250 kHz. For all boards, if the channel-gain list contains channel 16 only (the digital input channel), the maximum throughput is 3 MHz.

m. If using cascaded counter/timers, this value is 5 MHz.

n. Any two adjacent counter/timers, such as (1,2) or (2,3) or (3,4), can be cascaded. If you are not using cascaded counter/timers, this value is approximately 305.18 Hz.

o. High-edge and low-edge are supported for one-shot and repetitive one-shot modes. High-level and low-level are supported for event counting and rate generation modes.

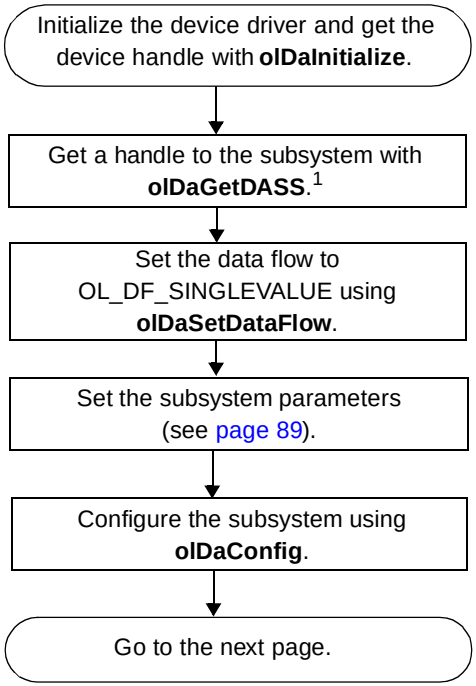
4

Programming Flowcharts

The following flowcharts show the steps required to perform data acquisition operations using DT-Open Layers. For illustration purposes, the DataAcq SDK functions are shown; however, the concepts apply to all DT-Open Layers software.

Note that many steps represent several substeps; if you are unfamiliar with the detailed operations involved with any one step, refer to the indicated page for detailed information. Optional steps appear in shaded boxes.

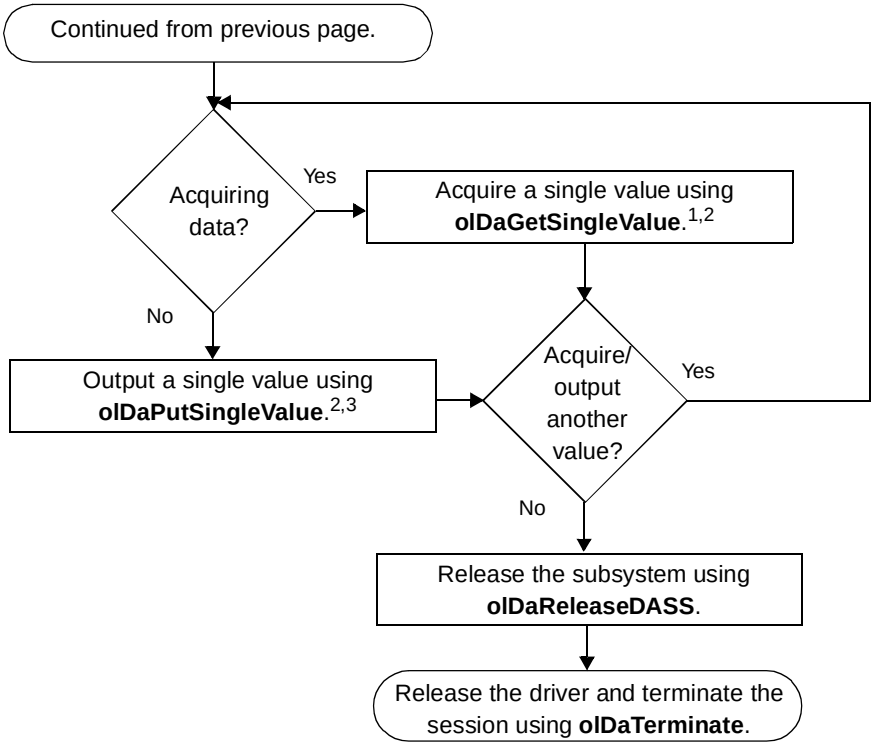
Single-Value Operations



Specify A/D for an analog input subsystem, D/A for an analog output subsystem, DIN for a digital input subsystem, or DOUT for a digital output subsystem.

[1] For DIN and DOUT functions, element 0 corresponds to Port A (lines 0 to 7), element 1 corresponds to Port B (lines 0 to 7), and element 2 corresponds to Port C (lines 0 to 6).

Single-Value Operations (cont.)

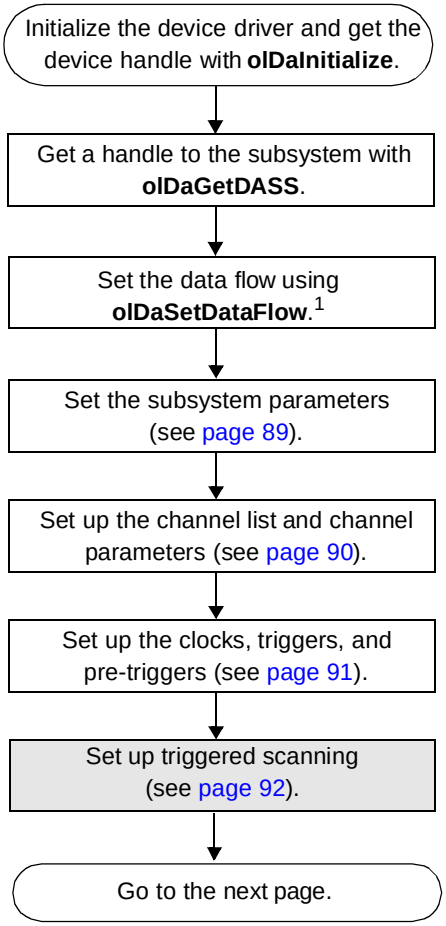


[1] Read a single analog input value or a digital input value from the specified channel/line. Analog input channels range from 0 to 15 for single-ended and pseudo-differential configurations or 0 to 7 for the differential configuration using the specified gain (1, 2, 4, or 8).

[2]The number of digital I/O lines depends on the resolution. If the resolution is 8, element 0 uses lines 0 to 7 (Port A) and element 1 uses lines 0 to 7 (Port B). If the resolution is 16, both element 0 and element 1 use lines 0 to 15 (Ports A and B), but both elements cannot be used at the same time. Element 2 always uses lines 0 to 6 (Port C).

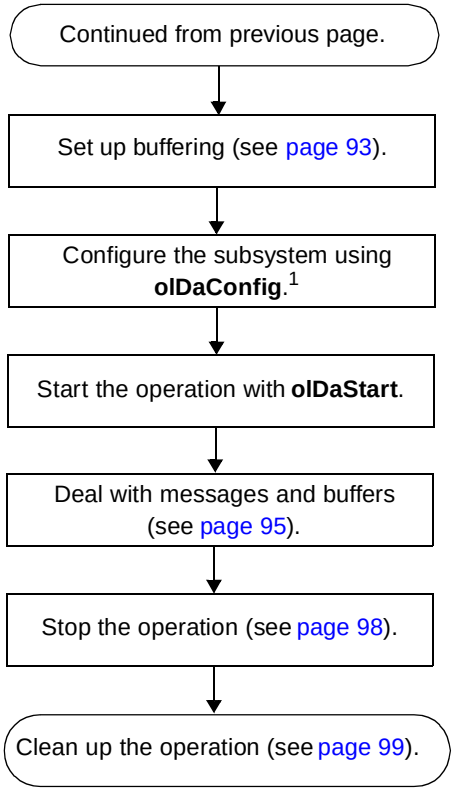
[3]The value is output to the specified analog output channel (DAC 0 or 1) or digital output line using a gain of 1.

Continuous A/D Operations



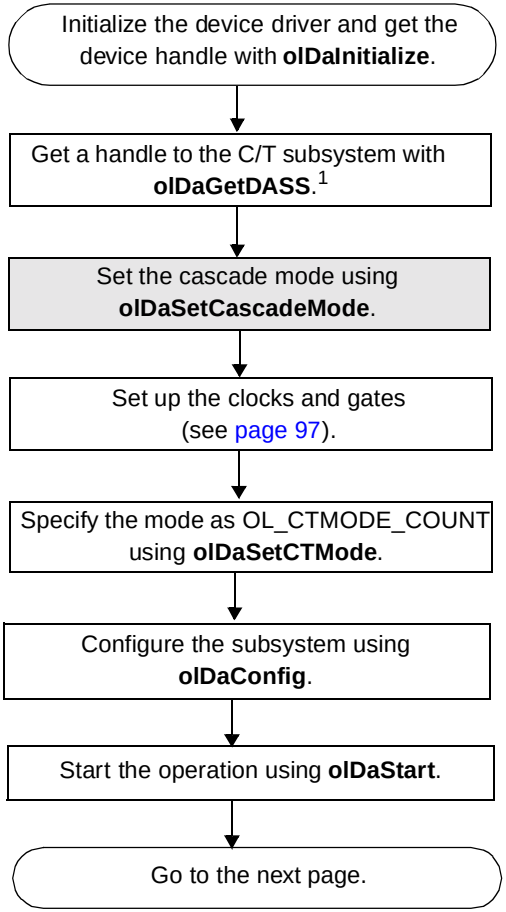
[1] Specify OL_DF_CONTINUOUS (the default value) for normal post-trigger operations, OL_DF_CONTINUOUS_PRETRIG for continuous pre-trigger operations, or OL_DF_CONTINUOUS_ABOUTTRIG for continuous about-trigger operations).

Continuous A/D Operations (cont.)



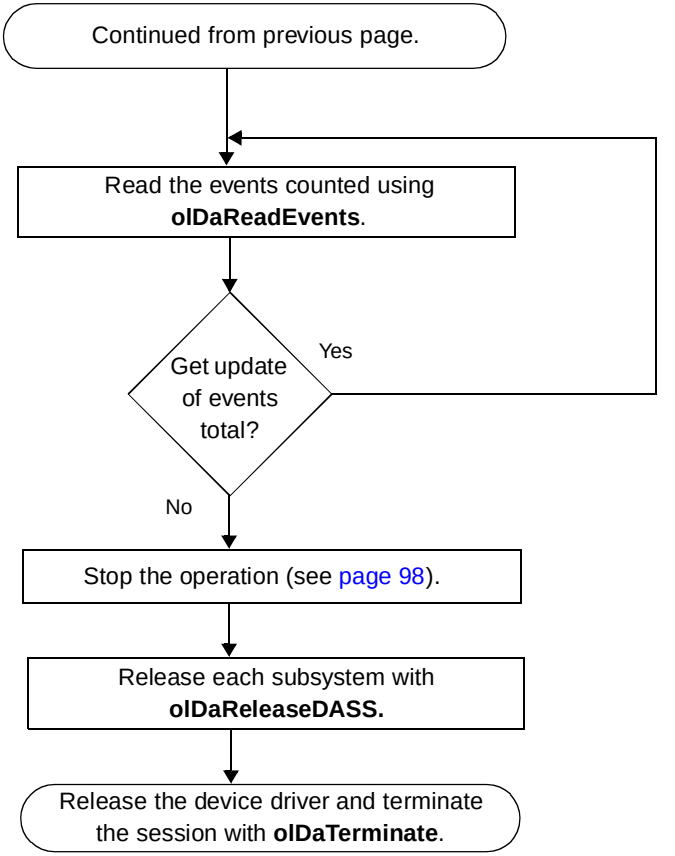
[1] After configuration, if using an internal clock, you can use **olDaGetClockFrequency** to get the actual frequency that the internal pacer clock could achieve; if using internal retrigger mode, you can use **olDaGetRetriggerFrequency** to get the actual frequency that the internal retrigger clock could achieve.

Event Counting Operations



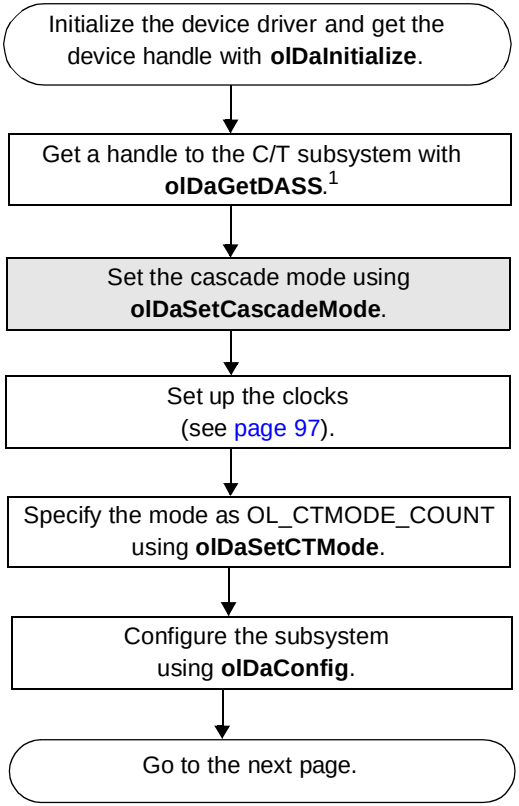
[1] Specify the appropriate C/T subsystem/element. The DT300 Series supports four elements (0, 1, 2, 3).

Event Counting Operations (cont.)



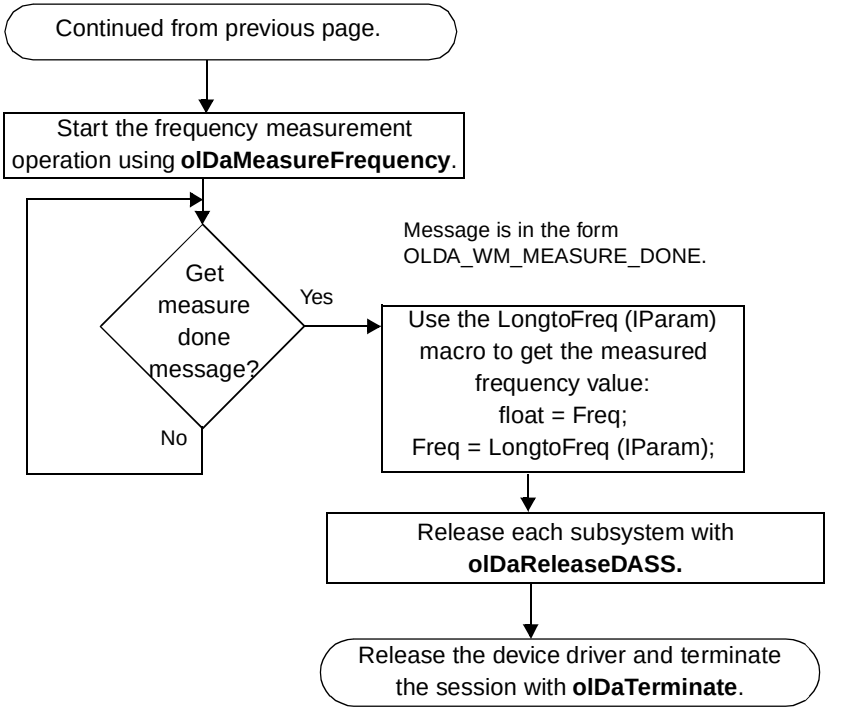
Frequency Measurement Operations

Note that this flowchart assumes that you are using the Windows system timer to generate the period over which the frequency is measured. If you need more accuracy the Windows timer provides, refer to page 51 and to the *DataAcq SDK User's Manual* for more information.

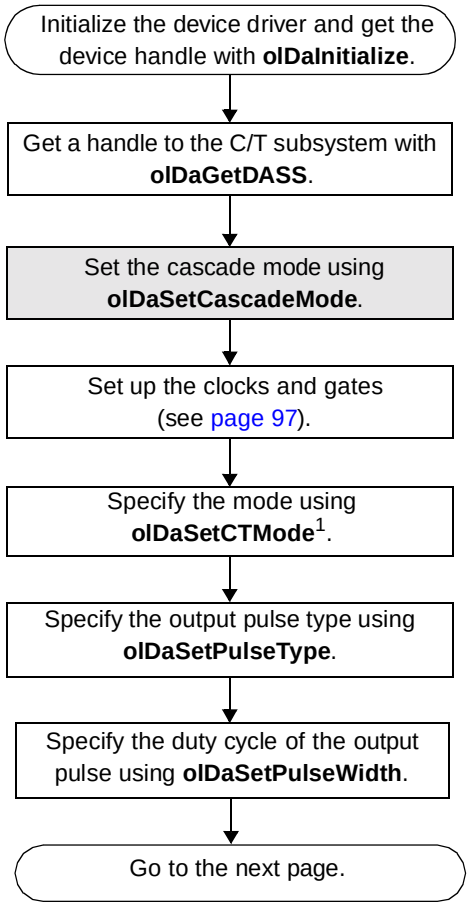


[1] Specify the appropriate C/T subsystem/element. The DT300 Series supports four elements (0, 1, 2, 3).

Frequency Measurement Operations (cont.)

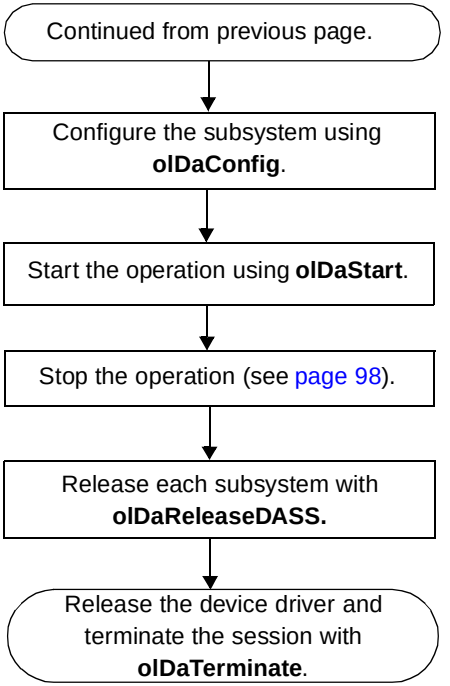


Pulse Output Operations



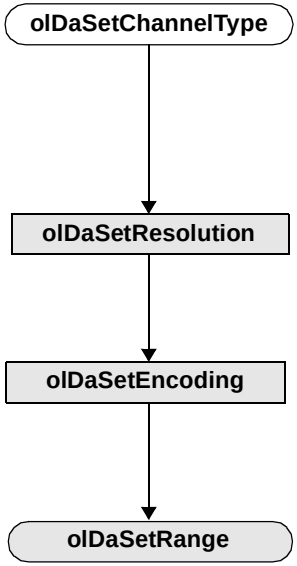
[1] Specify OL_CTMODE_RATE for rate generation (continuous pulse output), OL_CTMODE_ONESHOT for single one-shot, or OL_CTMODE_ONESHOT_RPT for repetitive one-shot.

Pulse Output Operations (cont.)



Note that this step is not needed for single one-shot operations.

Set Subsystem Parameters



Specify the channel type (single-ended or differential – differential is the default). Specify single-ended if you are using pseudo-differential channels (not needed for DIN and DOUT operations).

Required only for DIN and DOUT subsystems; specify a resolution of 8 (the default) to read/write eight lines at a time (Port A or Port B), or a resolution of 16 to read/write16 lines at a time (both Ports A and B). Port C has a fixed resolution of 7.

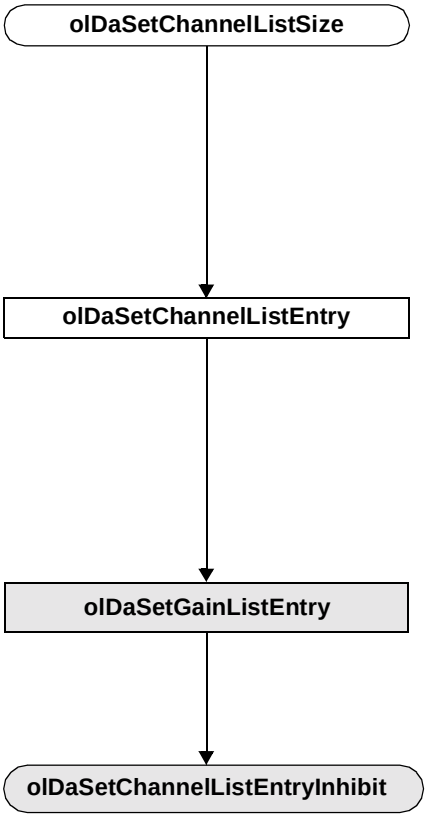
Specify the data encoding type as binary (OL_ENC_BINARY). This is the default value.

For the A/D subsystem, specify the voltage input range as either 0 to 10 V for unipolar signals or –10 V to +10 V (the default) for bipolar signals. For the DT321 and DT322 boards, the only supported input range is –10 V to +10 V. The input range and the gain determine the effective input range. See page 12 for more information.

For the D/A subsystem, specify the voltage output range as 0 to 10 V or 0 to 5 V for unipolar signals or as –10 V to +10 V or –5 V to +5 V for bipolar output signals. For the DT322 board, the only supported output range is –10 V to +10 V.

The step is unnecessary for DIN and DOUT subsystems.

Set Up Channel List and Channel Parameters



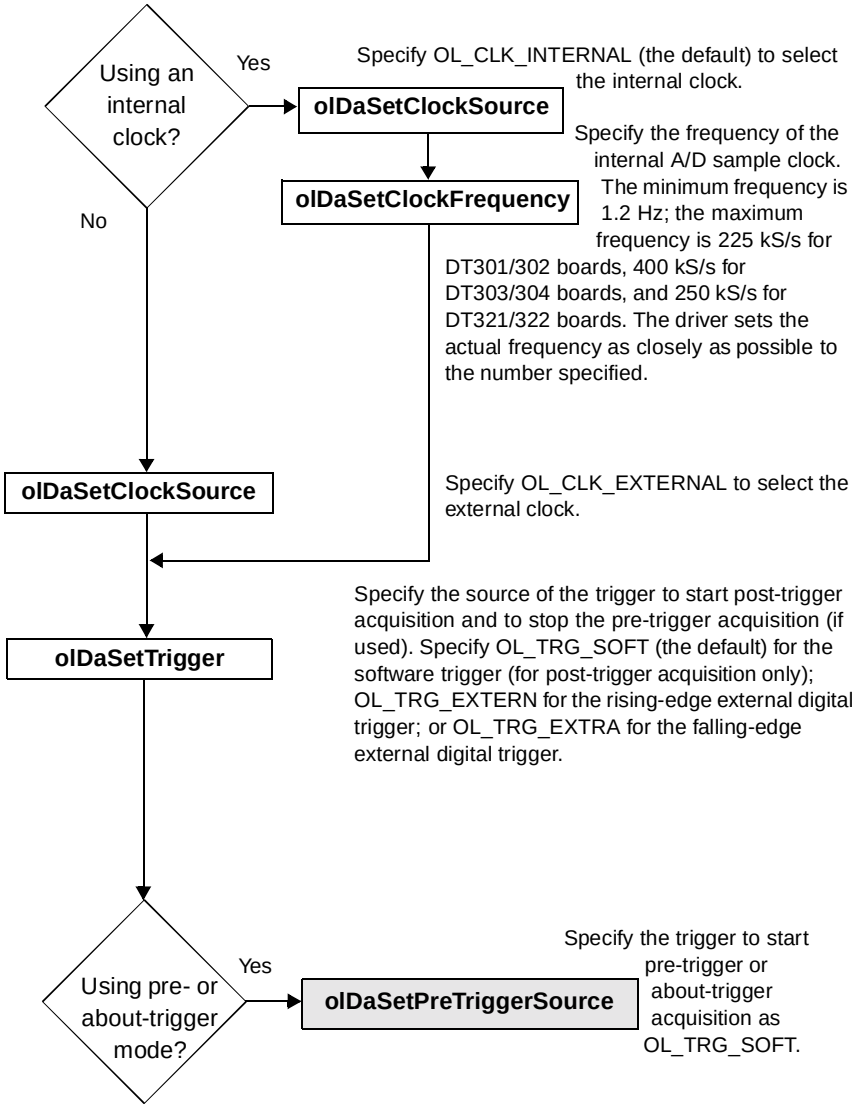
Specify the size of the analog input channel list, gain list, and channel inhibit lists (the default is 1; the maximum size is 1024).

Set up the analog input channel list. for the single-ended and pseudo-differential configuration, channels 0 to 15 are available; for the differential configuration, channels 0 to 7 are available.You can enter the digital input channel as channel 16 in the analog input channel list to achieve continuous digital input.

Specify the gain for each channel in the channel list (the gain list parallels the channel list). Gains 1,2,4, and 8 are supported for the A/D; use a gain of 1 (the default) if you use digital channel 16.

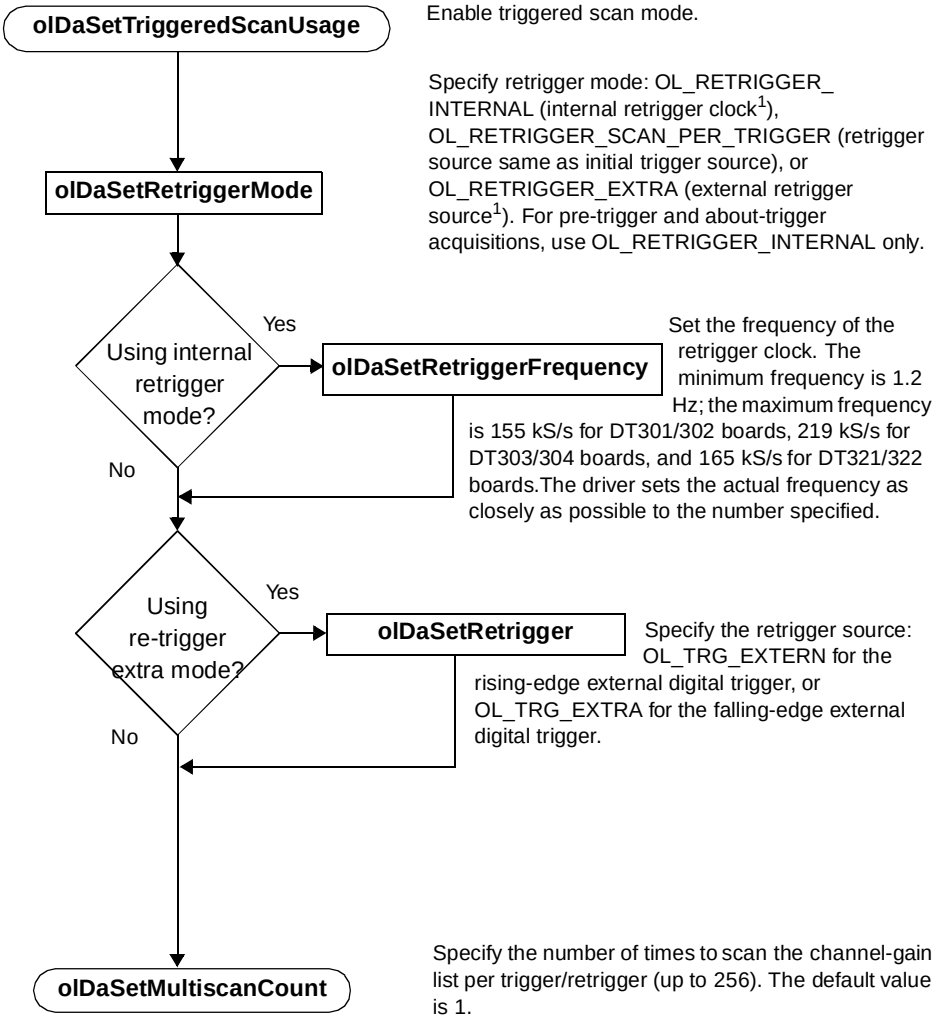
Enable or disable (the default) inhibition for the specified channel entries. If inhibited, the acquired values from the specified channels are discarded.

Set Clocks, Triggers, and Pre-triggers

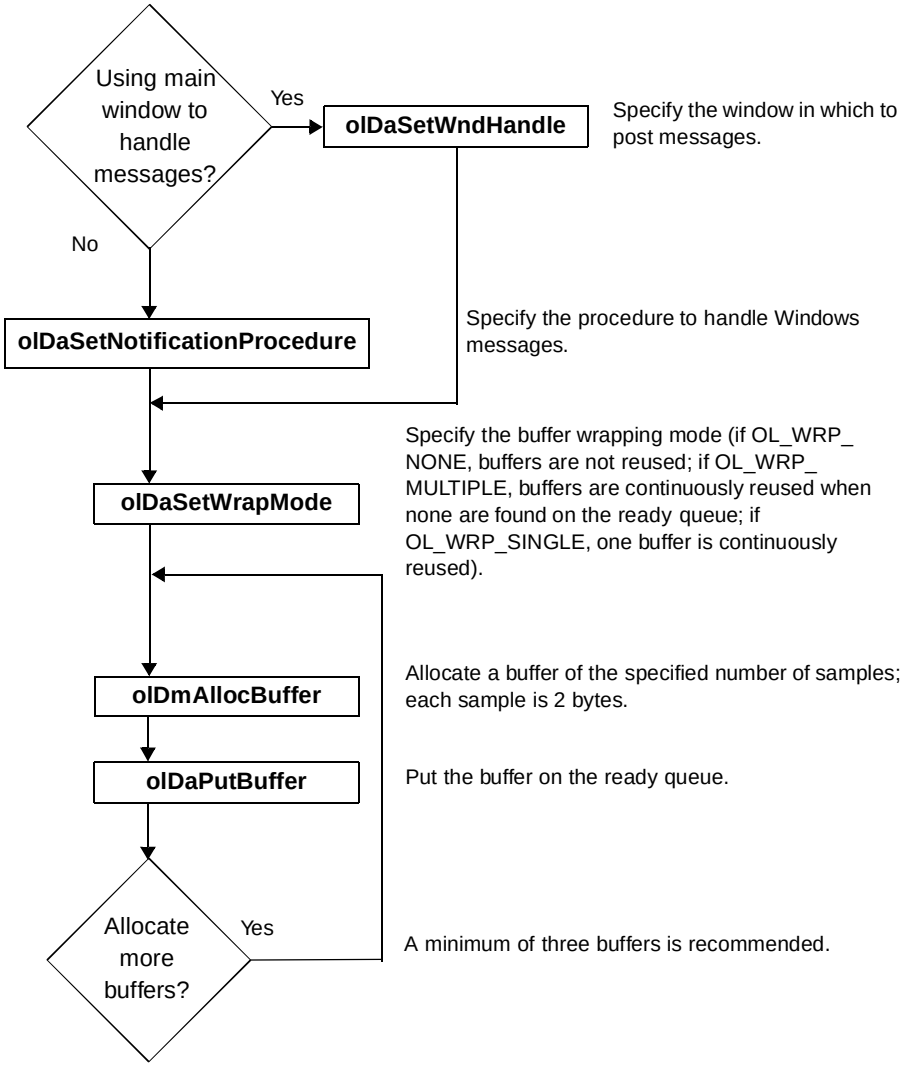


[1] The internal trigger can be set to anything.

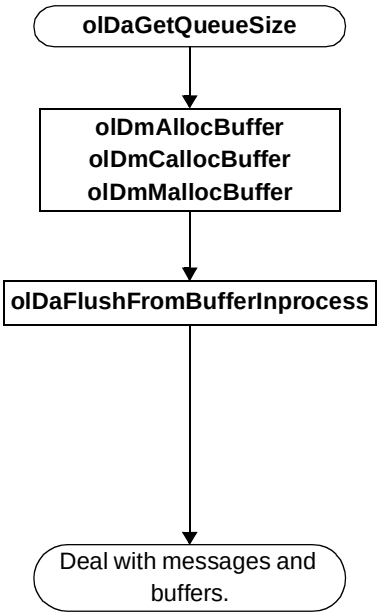
Set Up Triggered Scan



Set Up A/D Buffering



Transfer Data from an Inprocess Buffer



Determine the number of buffers on the inprocess queue (at least one must exist).

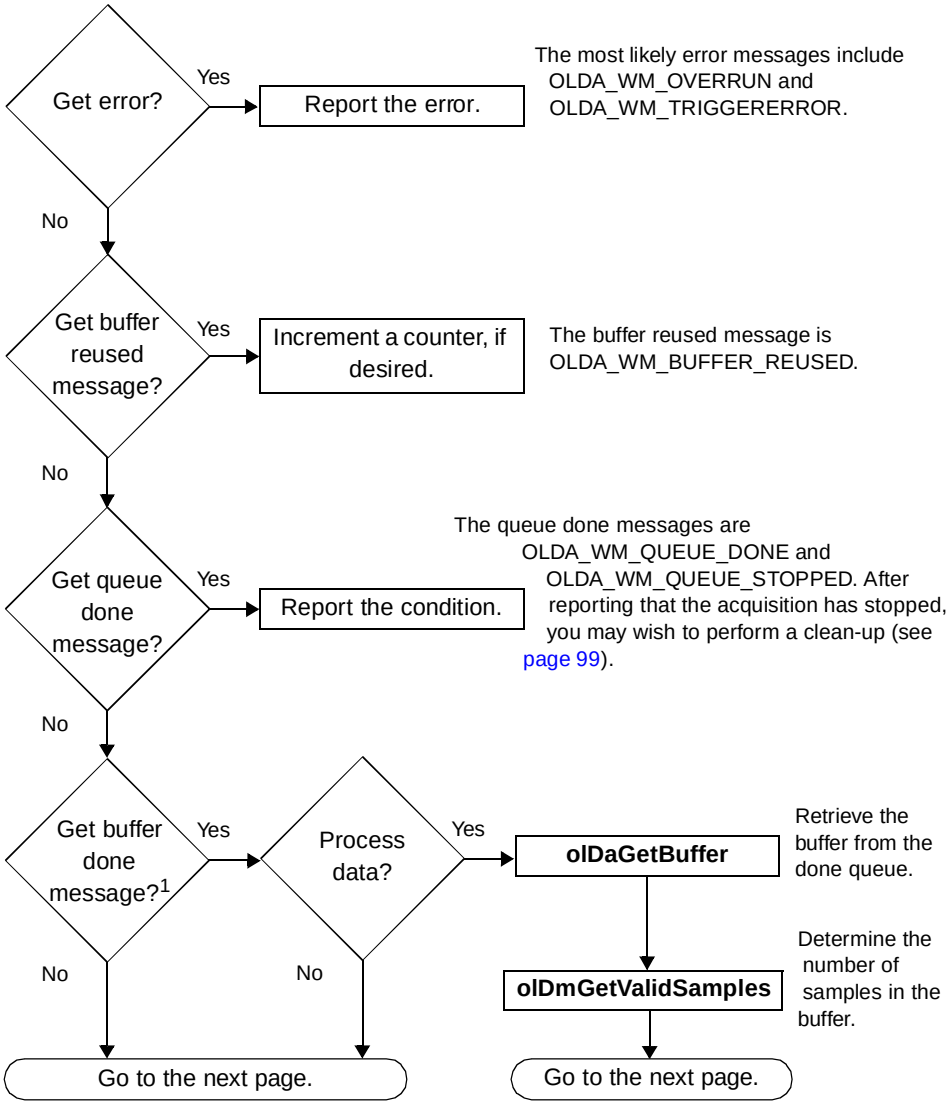
Allocate a buffer of the specified number of samples.

Copy the data from the inprocess buffer to the allocated buffer for immediate processing.

The buffer into which inprocess data was copied was put onto the done queue by the driver, resulting in an OLDA_WM_BUFFER_DONE message. See page 95 for more information.

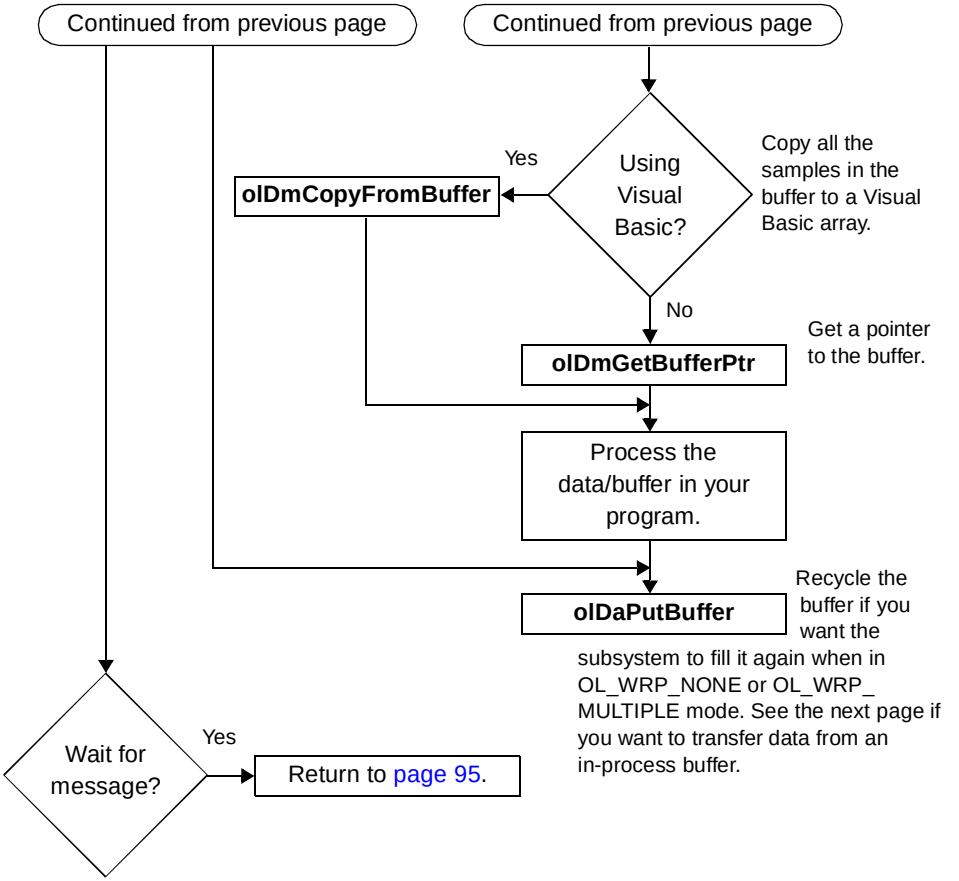
When the inprocess buffer has been filed, it too is placed on the done queue and an OLDA_WM_BUFFER_DONE message is posted. However, the number of valid samples is equal to the queue's maximum samples minus what was copied out.

Deal with A/D Messages and Buffers

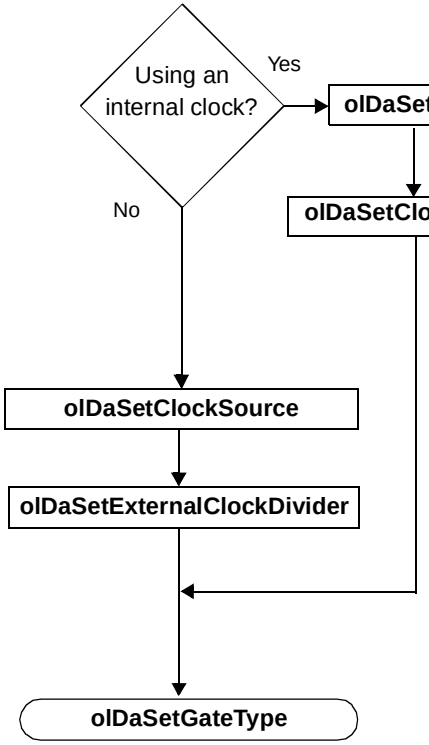


[1] The buffer done message is OLDA_WM_BUFFER_DONE or OLDA_WM_PRETRIGGER_BUFFER_DONE.

Deal with A/D Messages and Buffers (cont.)



Set Clocks and Gates for Counter/Timer Operations



Specify OL_CLK_INTERNAL (the default) to select the internal CT clock.

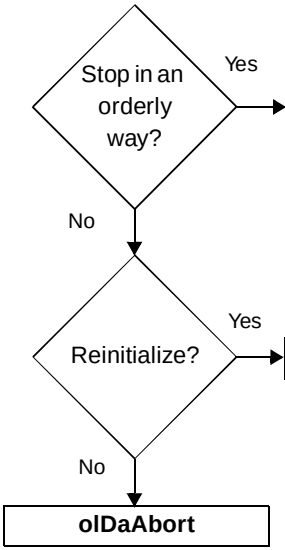
Specify the frequency of the output C/ pulse. The driver sets the actual frequency as closely as possible to the number specified.

Specify OL_CLK_EXTERNAL to select the external C/T clock.

Specify a clock divider of between 2.0 (the default) and 65536 to be applied to the externally-supplied input clock.

Specify one of the following gate types: Software (internal) (OL_GATE_NONE); High-Level (OL_GATE_HIGH_LEVEL); Low-Level (OL_GATE_LOW_LEVEL); High-Edge (OL_GATE_HIGH_EDGE); or Low-Edge (OL_GATE_LOW_EDGE).

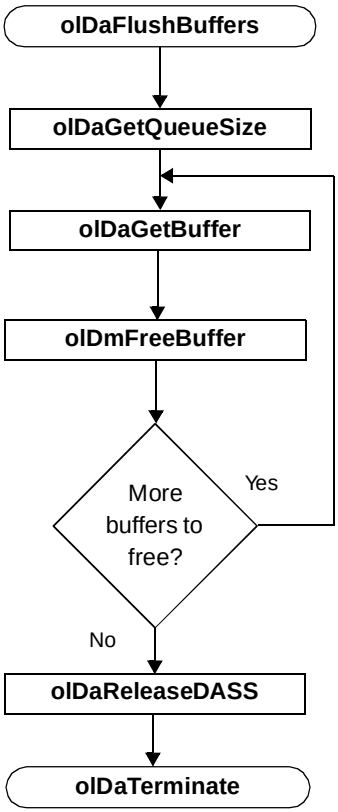
Stop the Operation



olDaStop stops the operation on the subsystem in the orderly way; the current inprocess buffers are filled or emptied and put on the done queue. The driver posts at least one buffer done and queue stopped message.

olDaAbort and **olDaReset** stop the operation on the subsystem immediately; the current buffers are not filled or emptied before they are put on the done queue. **olDaReset** also reinitializes the subsystem to a known state and flushes all buffers to the done queue.

Clean up the Operation



Flush all buffers on the ready and/or inprocess queues to the done queue.

Determine the number of buffers on the done queue.

Retrieve each buffer on the done queue.

Free each buffer retrieved from the done queue.

Release each subsystem.

Release the device driver and terminate the session.

5

Calibration

The DT300 Series boards are calibrated at the factory and should not require calibration for initial use. It is recommended that you check and, if necessary, readjust the calibration of the analog I/O circuitry on the DT300 Series boards every six months.

Note: Ensure that you installed the DT300 Series Device Driver and the DT300 Series Support Software prior to using the DT300 Series Calibration Utility. Refer to the *DT300 Series Getting Started Manual* for more information.

This chapter describes how to run the DT300 Series Calibration Utility and calibrate the analog I/O circuitry of the DT300 Series boards.

Running the Calibration Utility

To start the DT300 Series Calibration Utility, perform the following step:

1. Ensure that you installed the DT300 Series Support Software using the instructions in the *DT300 Series Getting Started Manual.*
2. Locate the DT300 Series program folder on your hard disk. *This program folder was created when you installed the DT300 Series device driver.*
3. Double-click the **Calibration Utility** icon in the program folder.

The main menu appears.

Once the DT300 Series Calibration Utility is running, you can calibrate the analog I/O circuitry, as described in the following sections.

Calibrating the Analog Input Subsystem

To calibrate the analog input circuitry, you need an external +9.3750 V reference (precision voltage source) available from vendors such as Electronic Development Corporation (EDC). Using an external +9.3750 V reference provides an accuracy of approximately ±3 LSB for the DT321 and DT322 boards and ±1 LSB for remaining DT300 Series boards.

You can also choose to calibrate the analog input circuitry automatically or manually; auto-calibration is the easiest to use and is the recommended calibration method.

The following sections describe how to configure for calibration using either of the supported references and how to calibrate the analog input circuitry automatically and manually.

Configuring for an External Reference

To calibrate the analog input circuitry using an external +9.3750 V reference, perform the following steps:

1. Connect Analog In 0 (TB1) to the positive side of the precision voltage source.
2. Connect Analog In 0 Return (TB2) to the negative side of the precision voltage source.
3. Connect Analog In 0 Return (TB2) to Analog Ground (TB18).
4. Connect Analog In 1 (TB3) to Analog In 1 Return (TB4) and to Analog Ground (TB18).

To calibrate the analog input circuitry automatically, continue on page 105; to calibrate the analog input circuitry manually, continue on page 106.

Using the Auto-Calibration Procedure

To calibrate the analog input subsystem automatically, perform the following steps:

1. From the main menu of the DT300 Series Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT300 Series board to configure from the combo box, then click **OK**.
3. From the main menu of the DT300 Series Calibration Utility, click **Calibrate**, then **A/D**.
4. In the Auto Calibration box, click **Go**.
   The bipolar (zero and full-scale) and unipolar (zero and full-scale) ranges are automatically calibrated.
5. Click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 108.

Note: Calibrating the PGH Zero setting in software is no longer required; the hardware calibrates this setting automatically.

If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Using the Manual Calibration Procedure

To calibrate the analog input circuitry manually, perform the following steps:

1. From the main menu of the DT300 Series Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT300 Series board to configure from the combo box, then click **OK**.
3. From the main menu of the DT300 Series Calibration Utility, click **Calibrate.**
4. Click **A/D**.
5. In the Range box, select **Bipolar**, then **Zero**.
6. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0 V (within 0.0001 V for the DT321 and DT322 boards and within 0.0010 V for the remaining DT300 Series boards).
7. In the Range box, select **Bipolar**, then **FS** (for full-scale).
8. Click the increment or decrement arrows in the Manual Adjustment box until the display reads +9.3750 V with the external reference (within 0.0001 V for the DT321 and DT322 boards and within 0.0010 V for the remaining DT300 Series boards).
9. In the Range box, select **Unipolar**, then **Zero**.
10. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0 V (within 0.0001 V for the DT321 and DT322 boards and within 0.0010 V for the remaining DT300 Series boards).
11. In the Range box, select **Unipolar**, then **FS** (for full-scale).
12. Click the increment or decrement arrows in the Manual Adjustment box until the display reads +9.3750 V with the external reference (within 0.0001 V for the DT321 and DT322

boards and within 0.0010 V for the remaining DT300 Series boards).

13. Click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 108.

Note: Calibrating the PGH Zero setting in software is no longer required; the hardware calibrates this setting automatically.

If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Calibrating the Analog Output Subsystem

To calibrate the analog output circuitry, use an external precision meter available from vendors such as Fluke.

The following sections describe how to configure for calibration using the supported meters and how to calibrate the analog output circuitry.

Configuring for an External Meter

To calibrate DAC0 using an external voltage meter, perform the following steps:

1. Connect Analog Out 0+ (TB19) to the positive side of the precision voltage meter.
2. Connect Analog Out 0 Return (TB20) to the negative side of the precision voltage meter.

To calibrate DAC1 using an external voltage meter, perform the following steps:

1. Connect Analog Out 1+ (TB23) to the positive side of the precision voltage meter.
2. Connect Analog Out 1 Return (TB22) to the negative side of the precision voltage meter.

Continue with the next section.

Using the Calibration Procedure

To calibrate the analog output circuitry, perform the following steps:

1. From the main menu of the DT300 Series Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT300 Series board to configure from the combo box, then click **OK**.
3. From the main menu of the DT300 Series Calibration Utility, click **Calibrate.**
4. Click **D/A**.
5. In the D/A box, select **DAC0**.
6. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0 V (within 0.0005 V).
7. Select **+FS** and verify that the display reads +9.375 V (within ±12 mV for the DT322 and within ±20 mV for the DT302 and DT304 boards.)
8. In the D/A box, select **DAC1**.
9. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0 V (within 0.0005 V).
10. Select **+FS** and verify that the display reads +9.375 V (within ±12 mV for the DT322 and within ±20 mV for the DT302 and DT304 boards.)
11. Click **Quit** when you are finished calibrating the analog output circuitry.

Once you have finished this procedure, the analog output circuitry is calibrated. To close the Calibration Utility, click the close box in the upper, right corner of the window.

6

Troubleshooting

General Checklist

Should you experience problems using a DT300 Series board, please follow these steps:

1. Read all the documentation provided for your product. Make sure that you have added any "Read This First" information to your manual and that you have used this information.
2. Check the Data Acquisition OMNI CD for any README files and ensure that you have used the latest installation and configuration information available.
3. Check that your system meets the requirements stated in the *DT300 Series Getting Started Manual.*
4. Check that you have installed your hardware properly using the instructions in the *DT300 Series Getting Started Manual.*
5. Check that you have installed and configured the device driver properly using the instructions in the *DT300 Series Getting Started Manual*.
6. Search the DT Knowledgebase in the Support section of the Data Translation web site (at www.datatranslation.com) for an answer to your problem.

If you still experience problems, try using the information in Table Table 8 to isolate and solve the problem. If you cannot identify the problem, refer to page 115.

Table 8: Troubleshooting Problems

Symptom	Possible Cause	Possible Solution
Board does not respond.	The board configuration is incorrect.	Check the configuration of your device driver to ensure that the board name and type are correct; see the instructions in the *DT300 Series Getting Started Manual*.
	The board is incorrectly aligned in a PCI expansion slot.	Check that the slot in which your DT300 Series board is located is a PCI slot and that the board is correctly seated in the slot; see the instructions in the *DT300 Series Getting Started Manual*.
	The board is damaged.	Contact Data Translation for technical support; refer to page 115.
Intermittent operation.	Loose connections or vibrations exist.	Check your wiring and tighten any loose connections or cushion vibration sources; see the instructions in the *DT300 Series Getting Started Manual*.
	The board is overheating.	Check environmental and ambient temperature; consult the board's specifications on page 129 of this manual and the documentation provided by your computer manufacturer for more information.
	Electrical noise exists.	Check your wiring and either provide better shielding or reroute unshielded wiring; see the instructions in the *DT300 Series Getting Started Manual*.

Table 8: Troubleshooting Problems (cont.)

Symptom	Possible Cause	Possible Solution
Data appears to be invalid.	An open connection exists.	Check your wiring and fix any open connections; see the instructions in the *DT300 Series Getting Started Manual*.
	A transducer is not connected to the channel being read.	Check the transducer connections; see the instructions in the *DT300 Series Getting Started Manual*.
	The board is set up for differential inputs while the transducers are wired as single-ended inputs or vice versa.	Check your wiring and ensure that what you specify in software matches your hardware configuration; see the instructions in the *DT300 Series Getting Started Manual*.
Computer does not boot.	Board is not seated properly.	Check that the slot in which your DT300 Series board is located is a PCI slot, that the board is correctly seated in the slot, and that the board is secured in the slot with a screw; see the instructions in the *DT300 Series Getting Started Manual*.
	The power supply of the computer is too small to handle all the system resources.	Check the power requirements of your system resources and, if needed, get a larger power supply; consult the board's specifications on page 122 of this manual.
System lockup.	Board is not seated properly.	Check that the slot in which your DT300 Series board is located is a PCI slot, that the board is correctly seated in the slot, and that the board is secured in the slot with a screw; see the instructions in the *DT300 Series Getting Started Manual*.

Service and Support

If you have difficulty using the DT300 Series board, Data Translation's Technical Support Department is available to provide prompt technical assistance. Support upgrades, technical information, and software are also available.

All customers can always obtain the support needed. The first 90 days are complimentary, as part of the product's original warranty, to help you get your system running. Customers who call outside of this time frame can either purchase a support contract or pay a nominal fee (charged on a per-incident basis).

For "priority support," purchase a support contract. Support contracts guarantee prompt response and are very affordable; contact your local sales office for details.

Refer to the Data Translation Support Policy located at the end of this manual for a list of services included and excluded in our standard support offering.

Telephone Technical Support

Telephone support is normally reserved for original warranty and support-contract customers. Support requests from non-contract or out-of-warranty customers are processed after requests from original warranty and support-contract customers.

For the most efficient service, please complete the form on page 117 and be at your computer when you call for technical support. This information helps to identify specific system and configuration-related problems and to replicate the problem in house, if necessary.

You can reach the Technical Support Department by calling (508) 481-3700 x1401.

If you are located outside the USA, call your local distributor. The name and telephone number of you nearest distributor are provided in your Data Translation catalog.

If you are leaving a message to request a support call, please include the following information:

- Your name (please include proper spelling),
- Your company or organization (please include proper spelling),
- A phone number,
- An email address where you can be reached,
- The hardware / software product you need help on,
- A summary of the issue or question you have,
- Your contract number, if applicable, and
- Your product serial number or purchase date.

Omitting any of the above information may delay our ability to resolve your issue.

Information Required for Technical Support

Name:_____Phone_____
Contract Number: _____
Address: _____
_____

Data Translation hardware product(s): _____
serial number: _____
configuration: _____
Data Translation device driver - SPO number: _____ _____
_____ version: _____
Data Translation software - SPO number:_____ _____
serial number: _____ version:_____
PC make/model: _____
operating system: _____ version:_____
Windows version: _____
processor: _____ speed:_____
RAM:_____ hard disk space:_____
network/number of users: _____ disk cache:_____
graphics adapter: _____ data bus:_____

I have the following boards and applications installed in my system:_____
_____
_____
I am encountering the following problem(s): _____
_____
_____
_____
and have received the following error messages/codes: _____
_____
_____
I have run the board diagnostics with the following results: _____
_____
You can reproduce the problem by performing these steps:
1. _____
_____
2. _____
_____
3. _____
_____

E-Mail and Fax Support

You can also get technical support by e-mailing or faxing the Technical Support Department:

- **E-mail**: You can reach Technical Support at the following address: tsupport@datx.com
  Ensure that you provide the following minimum information:

  – Your name,

  – Your company or organization,

  – A phone number,

  – An email address where you can be reached,

  – The hardware/software product you need help on,

  – A summary of the issue you are experiencing,

  – Your contract number, if applicable, and

  – Your product serial number or purchase date.

  Omitting any of the above information may delay our ability to resolve your issue.

- **Fax**: Please photocopy and complete the form on page 117, then fax Technical Support at the following number: (508) 481-8620.

Support requests from non-contract and out-of-warranty customers are processed with the same priority as telephone support requests.

World-Wide Web

For the latest tips, software fixes, and other product information, you can always access our World-Wide Web site free of charge at the following address: http://www.datatranslation.com

If Your Board Needs Factory Service

If your board must be returned to Data Translation, perform the following steps:

1. Record the board's serial number, then contact the Customer Service Department at (508) 481-3700 (if you are in the USA) and obtain a Return Material Authorization (RMA).

   If you are located outside the USA, call your local distributor for authorization and shipping instructions. The name and telephone number of your nearest distributor are listed in your Data Translation catalog.
   All return shipments to Data Translation must be marked with the correct RMA number to ensure proper processing.

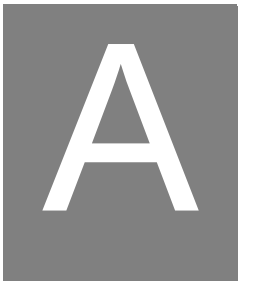
2. Using the original packing materials, if available, package the board as follows:

   – Wrap the board in an electrically conductive plastic material. Handle with ground protection. A static discharge can destroy components on the board.

   – Place in a secure shipping container.

3. Return the board to the following address, making sure the RMA number is visible on the outside of the box.

   Customer Service Dept.
   Data Translation, Inc.
   100 Locke Drive
   Marlboro, MA 01752-1192



Specifications

Table 9 lists the specifications for the A/D subsystem.

Table 9: A/D Subsystem Specifications

Feature	DT301/302 Specifications	DT303/304 Specifications	DT321/322 Specifications
Number of analog inputs Single-ended/ pseudo-differential: Differential:	16 8		
Number of gains	4 (1, 2, 4, 8)		
Resolution	12 bits	12 bits	16 bits
Data encoding	Offset binary		
System accuracy (full-scale) Gain = 1: Gain = 2: Gain = 4: Gain = 8:	 0.03% 0.04% 0.05% 0.05%	 0.03% 0.04% 0.05% 0.05%	 0.01% 0.02% 0.03% 0.03%
Nonlinearity (integral)	±1.0 LSB	±1.0 LSB	±4.0 LSB
Differential linearity	±0.5 LSB (no missing codes)	±0.5 LSB (no missing codes)	±1.2 LSB (no missing codes to 15 bits)
Range (V) Bipolar: Unipolar:	 ±1.25, 2.5, 5, 10 0 to 1.25, 0 to 2.5, 0 to 5, 0 to 10	 ±1.25, 2.5, 5, 10 0 to 1.25, 0 to 2.5, 0 to 5, 0 to 10	 ±1.25, 2.5, 5, 10

Table 9: A/D Subsystem Specifications (cont.)

Feature	DT301/302 Specifications	DT303/304 Specifications	DT321/322 Specifications
Drift Zero: Gain:	±30 µV+ (+20 µV * Gain)/°C ±30 ppm/°C	±30 µV+ (+20 µV * Gain)/°C ±30 ppm/°C	±25 µV+ (+10 µV*Gain)°C ±20 ppm/°C
Input impedance Off: On:	100 MΩ, 10 pF 100 MΩ, 100 pF		
Input bias current	±20 nA		
Common mode voltage	±11 V maximum (operational)		
Maximum input voltage	±40 V maximum (protection)		
A/D converter noise	0.3 LSB rms		
Amplifier input noise	20 µV rms + (10 µV rms*gain) 200 pA rms (current)	20 µV rms + (10 µV rms*gain) 200 pA rms (current)	15 µV rms + (10 µV rms*gain) 100 pA rms (current)
Channel-to-channel offset	±40.0 µV		
Channel acquisition time	3 µs	1 µs	1 µs
A/D conversion time	4.4 µs	2.5 µs	4 µs
Effective number of bits (ENOB)	11.5 bits	11.5 bits	13.5 bits
Total Harmonic Distortion	–80 dB typical	–80 dB typical	–90 dB typical
Channel crosstalk	–80 dB @ 1 kHz		

Table 9: A/D Subsystem Specifications (cont.)

Feature	DT301/302 Specifications	DT303/304 Specifications	DT321/322 Specifications
Data throughput			
Single analog channel:	225 kSamples/s (0.03% accuracy)	400 kSamples/s (0.03% accuracy)	250 kSamples/s (0.01% accuracy)
Multiple channels (scan):	225 kSamples/s (0.05% accuracy)	400 kSamples/s (0.05% accuracy)	250 kSamples/s (0.03% accuracy)
	200 kSamples/s (.03% accuracy)	360 kSamples/s (.03% accuracy)	150 kSamples/s (.01% accuracy)
Single digital channel:	3 MSamples/s	3 MSamples/s	3 MSamples/s
External A/D sample clock			
Input type:	Schmitt trigger, falling-edge sensitive		
Input load:	1 HCT14 (TTL)		
High-level input voltage:	2.0 V minimum		
Low-level input voltage:	0.8 V maximum		
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)		
High-level input current:	1.0 µA		
Low-level input current:	–1.0 µA		
Minimum pulse width:	100 ns (high); 100 ns (low)		
Maximum frequency:	See Data Throughput spec above		
Termination:	22 kΩ resistor pullup to +5 V		

Table 9: A/D Subsystem Specifications (cont.)

Feature	DT301/302 Specifications	DT303/304 Specifications	DT321/322 Specifications
External A/D digital (TTL) trigger			
Input type:	Schmitt trigger, edge sensitive		
Input load:	1 HCT14 (TTL)		
High-level input voltage:	2.0 V minimum		
Low-level input voltage:	0.8 V maximum		
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)		
High-level input current:	1.0 µA		
Low-level input current:	–1.0 µA		
Minimum pulse width:	100 ns (high); 100 ns (low)		
Termination:	22 kΩ resistor pullup to +5 V		

Table 10 lists the specifications for the D/A subsystem.

Table 10: D/A Subsystem Specifications

Feature	Specifications
Number of analog output channels (DT302, DT304, and DT322 only)	2
Resolution	
DT302, DT304:	12 bits
DT322:	16 bits
Data encoding (input)	Offset binary
Nonlinearity (integral)	
DT302, DT304:	±1 LSB
DT322:	±4 LSB
Differential linearity	
DT302, DT304:	±0.5 LSB (monotonic)
DT322:	±1 LSB (monotonic)

Table 10: D/A Subsystem Specifications (cont.)

Feature	Specifications
Output range DT302, DT304: DT322:	 ±10 V, 0 to 10 V, ±5 V, 0 to 5 V ±10 V
Zero Error:	Software-adjustable to zero
Gain Error DT302, DT304: DT322:	 ±2 LSB + reference ±6 LSB + reference
Current output	±5 mA minimum (10 V/ 2 kΩ)
Output impedance	0.3 Ω typical
Capacitive drive capability	0.001 µF minimum (no oscillations)
Protection	Short circuit to Analog Common
Power-on voltage	0 V ±10 mV maximum
Settling time to 0.01% of FSR	50 µs, 20 V step; 10.0 µs, 100 mV step
Slew rate	2 V/µs
Multiplying Zero Error	±10 mV maximum
External Reference Output	+10 V ±10 mV
Reference Input Impedance	5 kΩ typical

Table 11 lists the specifications for the DIN / DOUT subsystems.

Table 11: DIN/DOUT Subsystem Specifications

Feature	Port A Specifications	Port B Specifications	Port C Specifications
Number of lines	8 (bidirectional)	8 (bidirectional)	7 (bidirectional)
Termination	22 kΩ resistor pullup to +5 V; 22 Ω series resistor		
Inputs			
Input type:	Level sensitive	Level sensitive	Level sensitive
Input load:	2 FCT2574 (TTL)	2 FCT2574 (TTL)	1 ASIC (TTL)
High-level input voltage:	2.0 V minimum	2.0 V minimum	2.0 V minimum
Low-level input voltage:	0.8 V maximum	0.8 V maximum	0.8 V maximum
High-level input current:	3 µA	3 µA	100 µA
Low-level input current:	–3 µA	–3 µA	–100 µA
Outputs			
Output driver:	FCT2574 (TTL)	FCT2574 (TTL)	ASIC (TTL)
Output driver high voltage:	2.4 V minimum (IOH = –15 mA)	2.4 V minimum (IOH = –15 mA)	2.4 V minimum (IOH = 4 mA)
Output driver low voltage:	0.5 V maximum (IOL = 12 mA)	0.5 V maximum (IOL = 12 mA)	0.8 V maximum (IOL = 4 mA)

Table 12 lists the specifications for the C/T subsystems.

Table 12: C/T Subsystem Specifications

Feature	Specifications
Number of counter/timer channels	4
Clock Inputs	
Input type:	Schmitt trigger, rising-edge sensitive
Input load:	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum
Low-level input voltage:	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA
Low-level input current:	–1.0 µA
Minimum pulse width:	100 ns (high); 100 ns (low)
Maximum frequency:	5.0 MHz
Termination:	22 kΩ resistor pullup to +5 V
Gate Inputs	
Input type:	Schmitt trigger, level sensitive
Input load:	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum
Low-level input voltage:	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA
Low-level input current:	–1.0 µA
Minimum pulse width:	100 ns (high); 100 ns (low)
Termination:	22 kΩ resistor pullup to +5 V
Counter Outputs	
Output driver:	ALS244 (TTL)
Output driver high voltage:	2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA)
Output driver low voltage:	0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)
Termination:	22 Ω series resistor

Table 13 lists the power, physical, and environmental specifications for the DT300 Series board.

Table 13: Power, Physical, and Environmental Specifications

Feature	Specifications
Power	
+5 V (±0.25 V):	1.2 A nominal
– 5 V:	not used
+12 V:	55 mA maximum; 48 mA nominal
–12 V:	50 mA maximum; 38 mA nominal
+ 5 V Power Out (J1-1):	1 A maximum (with resettable fuse)
Physical	
Dimensions:	8.5 inches (length) by 4.2 inches (width)
Weight:	5.95 ounces (170 grams)
Environmental	
Operating temperature range:	0°C to 70°C
Storage temperature range:	–25°C to 85°C
Relative humidity:	To 95%, noncondensing

Table 14 lists the connector specifications for the DT300 Series board.

Table 14: Connector Specifications

Feature	Specifications
Connector part number	AMP, 68-pin, 0.05 Subminiature D, #749621-7
Shielded enclosure with jack screws	AMP #750752-1
Recommended shielded cable	Madison, 28 GA, Twisted Pair, #68KDK00029

Table 15 lists the specifications for the STP300 screw terminal panel.

Table 15: STP300 Specifications

Feature	Specifications
Mechanical	
J1:	AMP 68-pin connector, SCSI II (#787170-7)
J2:	AMP 26-pin connector (#104341-6)
Terminal block insulator:	Polyamide 6.6 GV
Screw type:	M 2.5 x 5, Chrome-plated steel
Wire size:	14 to 28 AWG
Dimensions:	4.9 inches (W) x 6.9 inches (L) x 0.90 inches (H) on 0.062 inches G10/FR4
Terminal material:	Nickel-plated brass
Board material:	FR4
Weight:	7 ounces
Mounting:	via four, 4-40 screws
Environmental:	
Storage temperature range:	–25°C to 85°C (derated operation)
Operational:	0°C to 55°C
Relative humidity:	To 95%, noncondensing

Table 16 lists the specifications for the cable EP305.

Table 16: EP305 Cable Specifications

Feature	Specifications
Length	2 meters
Conductors	34 twisted pairs, shielded, #28 AWG on 50 mil centers
Connectors	(1) AMP, 68-pin, self-locking receptacle, #787170-7

B

Connector Pin Assignments

Table 17 lists the pin assignments of connector J1 on the DT300 Series board.

Table 17: Pin Assignments for Connector J1 on the DT300 Series Boards

Pin Number	Signal Description	Pin Number	Signal Description
1	+ 5 V Output @1 A	2	User Clock Input 3
3	User Counter Output 3	4	External Gate 3
5	External Gate 1	6	User Counter Output 1
7	User Clock Input 1	8	Digital Ground
9	Digital I/O Port B, Line 7	10	Digital I/O Port B, Line 5
11	Digital I/O Port B, Line 3	12	Digital I/O Port B, Line 1
13	Digital I/O Port A, Line 7	14	Digital I/O Port A, Line 5
15	Digital I/O Port A, Line 3	16	Digital I/O Port A, Line 1
17	Digital Ground	18	Digital I/O Port C, Line 5
19	Digital I/O Port C, Line 3	20	Digital I/O Port C, Line 1
21	Digital Ground	22	External A/D Sample Clock In
23	Analog Output 1 Return	24	Analog Output 1
25	Analog Ground	26	Amp Low
27	Analog Input 15/7 Return	28	Analog Input 7
29	Analog Input 13/5 Return	30	Analog Input 5
31	Analog Input 11/3 Return	32	Analog Input 3
33	Analog Input 9/1 Return	34	Analog Input 1
35	Power Ground	36	User Clock Input 2
37	User Counter Output 2	38	External Gate 2
39	External Gate 0	40	User Counter Output 0

Table 17: Pin Assignments for Connector J1 on the DT300 Series Boards

Pin Number	Signal Description	Pin Number	Signal Description
41	User Clock Input 0	42	Digital Ground
43	Digital I/O Port B, Line 6	44	Digital I/O Port B, Line 4
45	Digital I/O Port B, Line 2	46	Digital I/O Port B, Line 0
47	Digital I/O Port A, Line 6	48	Digital I/O Port A, Line 4
49	Digital I/O Port A, Line 2	50	Digital I/O Port A, Line 0
51	Digital I/O Port C, Line 6	52	Digital I/O Port C, Line 4
53	Digital I/O Port C, Line 2	54	Digital I/O Port C, Line 0
55	Digital Ground	56	External A/D Trigger
57	Analog Output 0 Return	58	Analog Output 0
59	DAC1 Reference	60	DAC0 Reference
61	Analog Input 14/6 Return	62	Analog Input 6
63	Analog Input 12/4 Return	64	Analog Input 4
65	Analog Input 10/2 Return	66	Analog Input 2
67	Analog Input 8/0 Return	68	Analog Input 0

Table 18 lists the screw terminal assignments for connector J1 on the STP300 screw terminal panel.

Table 18: Pin Assignments for Connector J1 on the STP300

TB #	J1 Pin #	Description	TB #	J1 Pin #	Description
1	68	Analog Input 0	2	67	Analog Input 8/0 Return
3	34	Analog Input 1	4	33	Analog Input 9/1 Return
5	66	Analog Input 2	6	65	Analog Input10/2 Return
7	32	Analog Input 3	8	31	Analog Input 11/3 Return
9	64	Analog Input 4	10	63	Analog Input 12/4 Return
11	30	Analog Input 5	12	29	Analog Input 13/5 Return
13	62	Analog Input 6	14	61	Analog Input 14/6 Return
15	28	Analog Input 7	16	27	Analog Input 15/7 Return
17	26	Amp Low	18	25	Analog Ground
19	58	DAC0 Output	20	57	DAC0 Return
21	60	DAC0 Reference In and Out	22	23	DAC1 Return
23	24	DAC1 Output	24	59	DAC1 Reference In and Out
25	42	Digital Ground	26	41	User Clock Input 0
27	40	User Counter Output 0	28	39	External Gate 0
29	8	Digital Ground	30	7	User Clock Input 1
31	6	User Counter Output 1	32	5	External Gate 1
33	8	Digital Ground	34	36	User Clock Input 2
35	37	User Counter Output 2	36	38	External Gate 2
37	42	Digital Ground	38	2	User Clock Input 3

Table 18: Pin Assignments for Connector J1 on the STP300 (cont.)

TB #	J1 Pin #	Description	TB #	J1 Pin #	Description
39	3	User Counter Output 3	40	4	External Gate 3
41	1	+5 V Output @ 1 A	42	35	Power Ground
43	55	Digital Ground	44	55	Digital Ground
45	55	Digital Ground	46	56	External A/D Trigger
47	21	Digital Ground	48	22	External A/D Sample Clock Input
49	50	Digital I/O Port A, Line 0	50	16	Digital I/O Port A, Line 1
51	49	Digital I/O Port A, Line 2	52	15	Digital I/O Port A, Line 3
53	48	Digital I/O Port A, Line 4	54	14	Digital I/O Port A, Line 5
55	47	Digital I/O Port A, Line 6	56	13	Digital I/O Port A, Line 7
57	46	Digital I/O Port B, Line 0	58	12	Digital I/O Port B, Line 1
59	45	Digital I/O Port B, Line 2	60	11	Digital I/O Port B, Line 3
61	44	Digital I/O Port B, Line 4	62	10	Digital I/O Port B, Line 5
63	43	Digital I/O Port B, Line 6	64	9	Digital I/O Port B, Line 7
65	54	Digital I/O Port C, Line 0	66	20	Digital I/O Port C, Line 1

Table 18: Pin Assignments for Connector J1 on the STP300 (cont.)

TB #	J1 Pin #	Description	TB #	J1 Pin #	Description
67	53	Digital I/O Port C, Line 2	68	19	Digital I/O Port C, Line 3
69	52	Digital I/O Port C, Line 4	70	18	Digital I/O Port C, Line 5
71	51	Digital I/O Port C, Line 6	72	17	Digital Ground

Table 19 lists the screw terminal assignments for connector J2 on the STP300 screw terminal panel.

Table 19: Pin Assignments for Connector J2 on the STP300

Pin Number[a]	Description	Pin Number	Description
1	Analog Input 0	2	Analog Input 8
3	Analog Ground	4	Analog Input 9
5	Analog Input 1	6	Analog Ground
7	Analog Input 2	8	Analog Input 10
9	Analog Ground	10	Analog Input 11
11	Analog Input 3	12	Analog Ground
13	Analog Input 4	14	Analog Input 12
15	Analog Ground	16	Analog Input 13
17	Analog Input 5	18	Analog Ground
19	Analog Input 6	20	Analog Input 14

Table 19: Pin Assignments for Connector J2 on the STP300 (cont.)

Pin Number[a]	Description	Pin Number	Description
21	Analog Ground	22	Analog Input 15
23	Analog Input 7	24	Analog Ground
25	Amp Low	26	Not Connected

a. Signals Analog Input 8 to Analog Input 15 are not available on the 5B08 backplane.

Table 20 lists the screw terminal assignments for the STP68 and STP68-DIN screw terminal panel.

Table 20: Screw Terminal Assignments for the STP68 and STP68-DIN Screw Terminal Panel

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
1	1	+5 V Output @ 1 A	2	2	User Clock Input 3
3	3	User Counter Output 3	4	4	External Gate 3
5	5	External Gate 1	6	6	User Counter Output 1
7	7	User Clock Input 1	8	8	Digital Ground
9	9	Digital I/O Port B, Line 7	10	10	Digital I/O Port B, Line 5
11	11	Digital I/O Port B, Line 3	12	12	Digital I/O Port B, Line 1
13	13	Digital I/O Port A, Line 7	14	14	Digital I/O Port A, Line 5
15	15	Digital I/O Port A, Line 3	16	16	Digital I/O Port A, Line 1
17	17	Digital Ground	18	18	Digital I/O Port C, Line 5
19	19	Digital I/O Port C, Line 3	20	20	Digital I/O Port C, Line 1
21	21	Digital Ground	22	22	External A/D Sample Clock In

Table 20: Screw Terminal Assignments for the STP68 and STP68-DIN Screw Terminal Panel (cont.)

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
23	23	Analog Output 1 Return	24	24	Analog Output 1
25	25	Analog Ground	26	26	Amp Low
27	27	Analog Input 15/7 Return	28	28	Analog Input 7
29	29	Analog Input 13/5 Return	30	30	Analog Input 5
31	31	Analog Input 11/3 Return	32	32	Analog Input 3
33	33	Analog Input 9/1 Return	34	34	Analog Input 1
35	35	Power Ground	36	36	User Clock Input 2
37	37	User Counter Output 2	38	38	External Gate 2
39	39	External Gate 0	40	40	User Counter Output 0
41	41	User Clock Input 0	42	42	Digital Ground
43	43	Digital I/O Port B, Line 6	44	44	Digital I/O Port B, Line 4
45	45	Digital I/O Port B, Line 2	46	46	Digital I/O Port B, Line 0
47	47	Digital I/O Port A, Line 6	48	48	Digital I/O Port A, Line 4
49	49	Digital I/O Port A, Line 2	50	50	Digital I/O Port A, Line 0
51	51	Digital I/O Port C, Line 6	52	52	Digital I/O Port C, Line 4
53	53	Digital I/O Port C, Line 2	54	54	Digital I/O Port C, Line 0
55	55	Digital Ground	56	56	External A/D Trigger
57	57	Analog Output 0 Return	58	58	Analog Output 0
59	59	DAC1 Reference	60	60	DAC0 Reference
61	61	Analog Input 14/6 Return	62	62	Analog Input 6

Table 20: Screw Terminal Assignments for the STP68 and STP68-DIN Screw Terminal Panel (cont.)

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
63	63	Analog Input 12/4 Return	64	64	Analog Input 4
65	65	Analog Input 10/2 Return	66	66	Analog Input 2
67	67	Analog Input 8/0 Return	68	68	Analog Input 0

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Warranty and Service Policy

WARRANTY

Data Translation, for the effective period of the warranty set out below, warrants that its standard hardware products and software media will be free from defects in materials and workmanship under normal use and service. Data Translation's obligation under this warranty shall not arise until the Buyer returns the defective product, freight prepaid, to Data Translation's facility or another specified location. The only responsibility of Data Translation under this warranty is, at its option, to replace or repair, free of charge, any defective component part of such products.

EFFECTIVE PERIOD OF WARRANTY

All boards, modules, systems, and software media are warranted for one year from date of invoice. Products repaired or replaced within this warranty period maintain their original warranty. Products repaired or replaced outside the warranty period are warranted for 30 days from invoiced date of return.

RETURN OUTSIDE USA

Contact the local sales representative or factory for authorization and shipping instructions.

LIMITATIONS ON WARRANTY

The warranty set forth above does not extend to and shall not apply to

1. Products which have been repaired or altered by other than Data Translation personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Data Translation.
2. Products which have been subject to misuse, neglect, accident, or improper installation.

THE WARRANTY AND REMEDIES SET FORTH ABOVE ARE IN LIEU OF ALL OTHER WARRANTIES EXPRESSED OR IMPLIED, ORAL OR WRITTEN, EITHER IN FACT OR BY OPERATION OF LAW, STATUTORY OR OTHERWISE, INCLUDING WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE WHICH DATA TRANSLATION SPECIFICALLY DISCLAIMS. DATA TRANSLATION, INC. NEITHER ASSUMES NOR AUTHORIZES ANY OTHER LIABILITY IN CONNECTION WITH THE SALES, INSTALLATION, OR USE OF ITS PRODUCTS. DATA TRANSLATION, INC. SHALL HAVE NO LIABILITY FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND ARISING OUT OF THE SALE, INSTALLATION, OR USE OF ITS PRODUCTS.

CUSTOMER SERVICE POLICY

a. Data Translation, Inc. will repair or replace, at its option, any faulty item within ten days after receipt of said part regardless of its warranty status.

b. A Quick Turnaround Plan is available to expedite servicing. Contact the Data Translation Customer Service Department for details.

c. If a product should fail during the warranty period, it will be repaired free of charge. For out-of-warranty repairs, the customer will be invoiced for repair charges.

RETURN/REPAIR PROCEDURES

Upon determining that repair services are required, or to return a product to Data Translation, contact the Data Translation Customer Service Department at (508) 481-3700, extension 394 to obtain a Return Material Authorization (RMA) number. Have the following information ready when you call: complete product model number, product serial number, name, address, and telephone number of person returning product; and any special repair instructions.

Carefully package the product in anti-static packaging, making sure the RMA number appears on the outside of the package. Ship prepaid to:

Customer Service Department
Data Translation, Inc.
100 Locke Drive
Marlboro, MA 01752-1192 USA

On completion of required service, an invoice is issued stating charges, when applicable, and the work that has been completed.

Data Translation Support Policy

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Maintenance Release means a new release of any Product that contains corrections to previously identified errors. Maintenance Releases are designated in the hundredths digit of the release designation (e.g., 1.2.2 is a Maintenance Release from 1.2.1).

Major Release means a new version of any Product that involves major feature changes. Major Releases are designated in the ones digit of the release designation (e.g., 2.0, 3.0, etc., are Major Releases).

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(a) problem reporting, tracing and monitoring by internet electronic mail; (b) telephone support for problem determination, verification and resolution (or instruction as to work-around, as applicable) on a call-back basis during Data Translation's normal weekday business hours of 8:30 a.m. to 5 p.m. Eastern Time, excluding holidays; (c) one (1) copy of each Maintenance Release for the Products comprising the Software; (d) commercially reasonable efforts to diagnose and resolve defects and errors in the Software and Documentation; and (e) furnishing of the maintenance and technical support described above, for the current release and the immediately previous Enhanced Release of the Software. Support Services will be delivered in English. Enhanced Releases and Major Releases can be purchased by Licensee at a discount of twenty five percent (25%) off the then-current list prices for such releases.

3. EXCLUSIONS. Support Services do not include: (a) the provision of or support for Products other than those identified in the Agreement as to which the applicable license and support fees shall have been paid, including without limitation, compilers, debuggers, linkers or other third party software or hardware tools or components used in conjunction with any Product; (b) services required as a result of neglect, misuse, accident, relocation or improper operation of any Product or component thereof, or the failure to maintain proper operating and environmental conditions; (c) support for processors other than Licensed Processors or for Products modified by or on behalf of Licensee; (d) repair or restoration of any Software arising from or caused by any casualty, act of God, riot, war, failure or interruption of any electrical power, air conditioning, telephone or communication line or any other like cause.

It is Licensee's responsibility to have adequate knowledge and proficiency with the use of the compilers and various software languages and operating systems used with the Products, and this Support Policy does not cover training of, or detailed direction on the correct use of these compilers, operating systems, or components thereof. On-site

assistance shall not be provided hereunder, but may be available on a per call basis at Data Translation's then current rates (Specialized Application Support Charges) for labor, travel time, transportation, subsistence and materials during normal business hours, excluding holidays observed by Data Translation. The troubleshooting of faulty Licensee programming logic may also be subject to Specialized Application Support Charges and is not covered under this Support Policy. Direct authoring or development of customized application code is not provided hereunder but may be available on a per call basis upon payment of Specialized Application Support Charges.

4. LICENSEE'S OBLIGATIONS. Licensee agrees: (a) that the Designated Contact persons identified on the Support Order Form (or such other replacement individuals as Licensee may designate in writing to Data Translation) shall be the sole contacts for the coordination and receipt of the Support Services set forth in Section 2 of this Support Policy; (b) to maintain for the term of the support, an internet address for electronic mail communications with Data Translation; (c) to provide reasonable supporting data (including written descriptions of problems, as requested by Data Translation) and to aid in the identification of reported problems; (d) to install and treat all software releases delivered under this Support Policy as Software in accordance with the terms of the Agreement; and (e) to maintain the Agreement in force and effect.

5. TERM AND TERMINATION.

5.1 Term. For each Product comprising the Software, Support Services will begin on the later of the date the Software warranty granted in the Agreement expires or the date of Licensee's election to obtain Support Services and will apply to such Product for an initial term of one (1) year, unless an alternative commencement date is identified in the Support Order Form. The initial term will automatically be extended for additional terms of one (1) year unless Support Services are terminated at the expiration of the initial term or any additional term, by either party upon thirty (30) days prior written notice to the other party.

5.2 Default. If Licensee is in default of its obligations under the Agreement (except for Licensee's obligation to maintain valid licenses for the Software, in which case termination is immediate) and such default continues for thirty (30) days following receipt of written notice from Data Translation, Data Translation may, in addition to any other remedies it may have, terminate the Support Services.

6. CHARGES, TAXES AND PAYMENTS.

6.1 Payment. The Support Fee in respect of the initial term, and, as adjusted pursuant to Section 5.2 in respect of additional terms, is payable in full prior to the commencement of the initial term or any additional term, as applicable.

6.2 Changes From Term to Term. The Support Fee and the terms and conditions of this Support Policy may be subject to change effective at the end of the initial term or any additional term by giving Licensee at least sixty (60) days prior written notice.

6.3 Taxes. The charges specified in this Support Policy are exclusive of taxes. Licensee will pay, or reimburse Data Translation, for all taxes imposed on Licensee or Data Translation arising out of this Support Policy except for any income tax imposed on Data Translation by a governmental entity. Such charges shall be grossed-up for any withholding tax imposed on Data Translation by a foreign governmental entity.

6.4 Additional Charges. Licensee agrees that Data Translation or its authorized distributor will have the right to charge in accordance with Data Translation's then-current policies for any services resulting from (a) Licensee's modification of the Software, (b) Licensee's failure to utilize the then-current release, or the immediately previous Enhanced Release, of

the Software, (c) Licensee's failure to maintain Data Translation Support Services throughout the term of the Agreement, (d) problems, errors or inquiries relating to computer hardware or software other than the Software, or (e) problems, errors or inquiries resulting from the misuse or damage or of the Software or from the combination of the Software with other programming or equipment to the extent such combination has not been authorized by Data Translation. Pursuant to Section 2.4 of the Agreement, the Support Fee will also be adjusted in accordance with Data Translation's then current fee schedule as additional Licensed Processors are added. Support Fees do not include travel and living expenses or expenses for installation, training, file conversion costs, optional products and services, directories, shipping charges or the cost of any recommended hardware, third party software, or third party software maintenance fees or operating system upgrade.

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